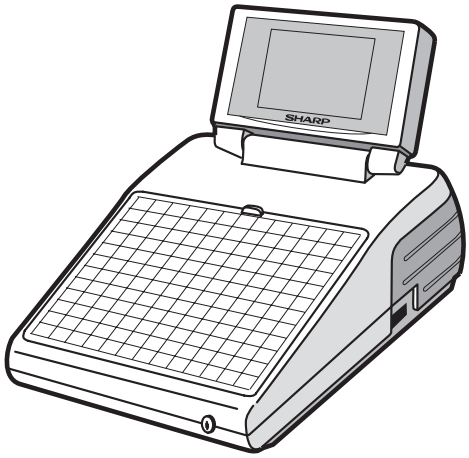
ER-A770VS

SHARP SERVICE MANUAL

CODE : 00ZERA770VSME



MODEL ER-A770

(For "V" version)

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PARTS GUIDE

Parts marked with "⚠" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

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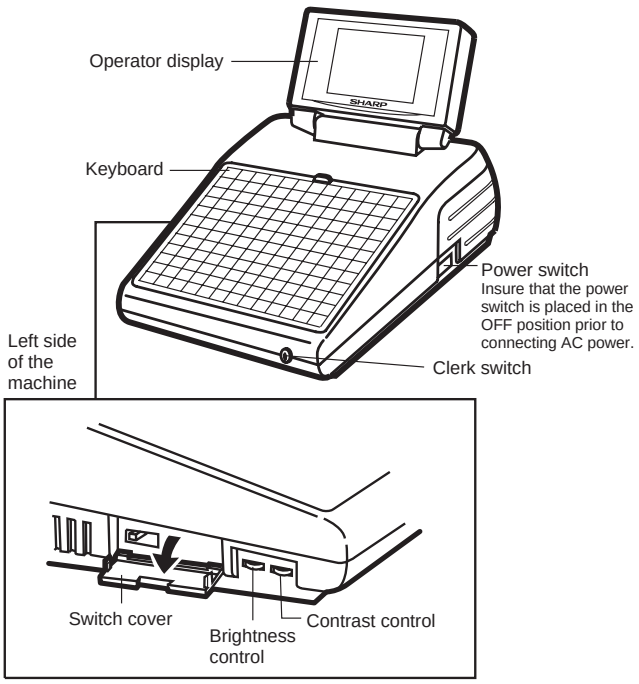
The contents are subject to change without notice.

CHAPTER 1. SPECIFICATION

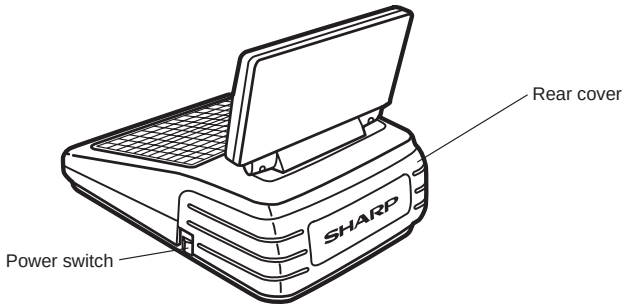
1. Apearance

External view

Front view



Rear view



2. Rating

External dimensions	290 (W) × 365 (D) × 282 (H) mm
Weight	5.5 kg
Power source	Official voltage and frequency
Power consumption	Stand-by: 26W Operating: 32W (max.)
Working temperatures	0 to 40 °C

3. Keyboard

1) Standard keyboard layout

MODE	GC RCPT	SLIP	AUTO 2	L1	12	24	36	48	60	72	84	96
TEXT 4	TEXT 5	TEXT 6	AUTO 1	L2	11	23	35	47	59	71	83	95
TEXT 1	TEXT 2	TEXT 3	GUEST #	L3	10	22	34	46	58	70	82	94
TRANS OUT	TRANS IN	BS	BT	VAT SHIFT	9	21	33	45	57	69	81	93
MISC FUNC	CANCEL	ENTER	VOID	RF	8	20	32	44	56	68	80	92
PAGE UP	↑	PAGE DOWN	PRICE SHIFT3	WITH	7	19	31	43	55	67	79	91
←	↓	→	PRICE SHIFT2	WITH OUT	6	18	30	42	54	66	78	90
⊗	•	CL	PRICE SHIFT1	OPENED GLU	5	17	29	41	53	65	77	89
7	8	9	PLU/ SUB	GLU	4	16	28	40	52	64	76	88
4	5	6	CH #	NBAL	3	15	27	39	51	63	75	87
1	2	3	CR #	FINAL	2	14	26	38	50	62	74	86
00	0	000	ST	TL	1	13	25	37	49	61	73	85

2) Key top name

① Standard key top

KEY TOP	DESCRIPTION
0 ~ 9,000,00	Numeric keys
•	Decimal point key
CL	Clear key
⊗	Multiplication key
VAT SHIFT	Value-added tax shift key
RF	Refund key
VOID	Void key
PLU / SUB	Price lookup / Subdepartment key
1 ~ 96	Direct price look up key
L1 ~ L3	PLU level shift 1 ~ 3 keys
FINAL	Tentative finalization key
MISC FUNC	Miscellaneous function key
MODE	Mode menu key
ENTER	Enter key
AUTO1,2	Automatic sequencing 1 and 2 keys
CR#	Credit menu key
CH#	Check menu key
ST	Subtotal key
TL	Total key
PAGE UP	Page up key
PAGE DOWN	Page down key
→	Cursor right key
←	Cursor left key
↑	Cursor up key
↓	Cursor down key
CANCEL	Cancel key
WITH	With key
WITH OUT	Without key
TEXT1 ~ 6	Direct text 1 ~ 6 keys
PRICE SHIFT 1 ~ 3	Price level shit 1 ~ 3 keys
GC RCPT	Guest check receipt key
GUEST #	Guest number entry key
OPENED GLU	Opened GLU list key
GLU	Guest lookup key
NBAL	New balance key
TRANS OUT	Transfer out key
TRANS IN	Transfer in key

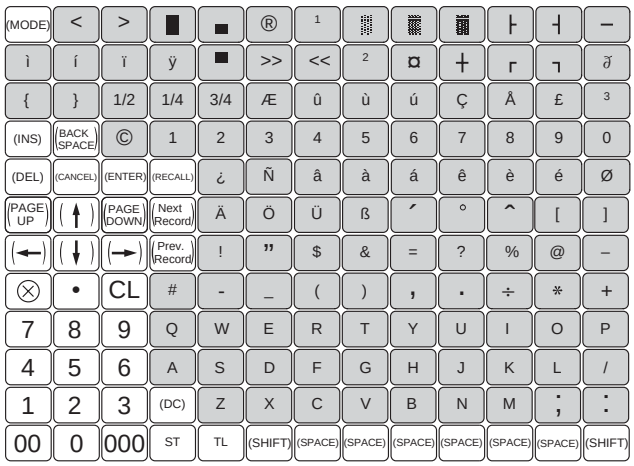
KEY TOP	DESCRIPTION
SLIP	Slip print key
BS	Bill separation key
BT	Bill totalize / Bill transfer key

② Optional key top

KEY TOP	DESCRIPTION
97 ~ 135	Direct price look up keys
1 ~ 99	Department keys
%1 ~ %9	Percent 1 ~ 9 keys
⊖1 ~ ⊖9 keys	Discount 1 ~ 9 keys
CR1 ~ CR8	Credit 1 ~ 8 keys
CA2	Cash total 2 key
RA1,RA2	Received on account 1 and 2 keys
PO1,PO2	Paid out 1 and 2 keys
AUTO3 ~ AUTO25	Automatic sequencing 3 ~ 25 keys
CH1 ~ CH4	Check 1 ~ 4 keys
CASH TIP	Cash tip key
TIP PAID	Tip paid key
#	Non-add code entry key
NS	No-sale key
MGR#	Manager code entry key
OPEN TARE	Tare entry Key
REPEAT	Repeat entry key
PERSON#	Person number entry key
IND. PAYMENT	Individual payment key
RCP. SW	Receipt ON / OFF key
SCALE	Scale entry key
TEXT 7 ~ 40	Text 7 ~ 40 keys
EX1 ~ 9	Foreign currency exchange 1 ~ 9 keys
AMT	Amount entry key
DRV NC	New check 2 key (For drive-thruogh)
DRV GLU	Guest look up 2 key (For drive-through)
VAT	Value-added tax key
NON-CASH TIP	Non-cash tip key
1/2	1/2 key
CLERK#	Clerk code entry key
RCPT	Receipt print key
PINT	Pint key
DEPO(+)	Deposit plus entry key
DEPO(–)	Deposit minus entry key
TEXT#	Text number key
EMP#	Employee key
TIME IN	Time in key
SBTL VOID	Subtotal void key
TIME OUT	Time out key
BREAK IN/OUT	Break in/out key
VP	Validation print key
RTN	Return key
DEPT SHIFT 1 ~ 4	Department shift 1 ~ 4 keys
DIFFER ST	Difference subtotal key
C.BILL	Cumulated bill key
GC COPY	Guest check copy key
EX#	Foreign currency exchange menu key
VIP	VIP sale key
H.T.	Hotel transfer key
CLK1 ~ 10	Clerk entry 1 ~ 10 keys
CHECK PRINT	Check print key
BACK SPACE	Back space key
DEL	Delete key
L4 ~ L10	PLU level shift 4 through 10 keys

KEY TOP	DESCRIPTION
PRICE SHIFT 4 ~ PRICE SHIFT 7	Price level shift 4 through 7 keys
PLU MENU 01 ~ PLU MENU 50	PLU menu 1 through 50 keys
WASTE	WASTE mode key
WAIT	WAIT mode key (for drive-thru)
RECALL	Re-call key (for drive thru)
C_NEXT	Condiments next key
D_DISP	Drive-thru menu key
E. BILL	Entertainment bill key
RC TTL	Recall TOTAL STATUS key

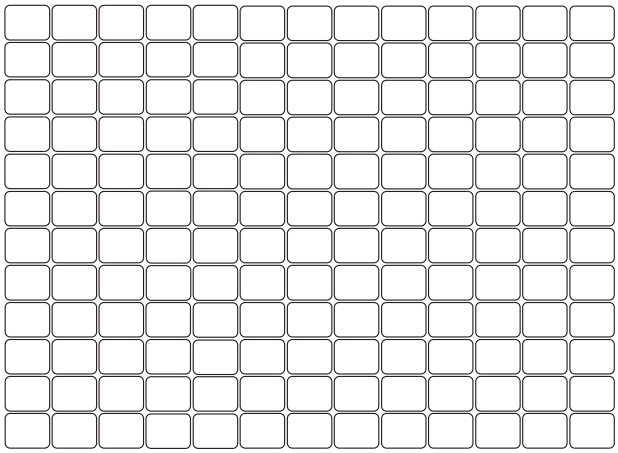
3) Text programming key sheet layout



: The shaded area contains the character keys which are used for programming characters.

KEY TOP	DESCRIPTION
SHIFT	Used for programming characters. For more information about programming characters, see the section "How to Enter Alphanumeric Characters."
DC	
INS	
DEL	
BACK SPACE	
[→], [←], [↑], [↓]	Used to move the cursor.
ENTER	Used to program each setting.
TL	Used to finalize programming.
CANCEL	Used to cancel programming and to get back to the previous screen.
MODE	Used for changing the operating mode.
PREV RECORD	Used to go back to the previous record, e.g., from the department 2 programming window back to the department 1 programming window.
NEXT RECORD	Used to go to the next record, for example, in order to program unit prices for sequential departments.
PAGE DOWN	Used to scroll the window to go to the next page.
PAGE UP	Used to scroll the window to go back to the previous page.
CL	Used to clear the last setting you have programmed or clear the error state.
•	Used to toggle between two or more options.
ST	Used to list those options which you can toggle by the [•] key.
RECALL	Used to call up a desired code.
Numeric keys	Used for entering figures.

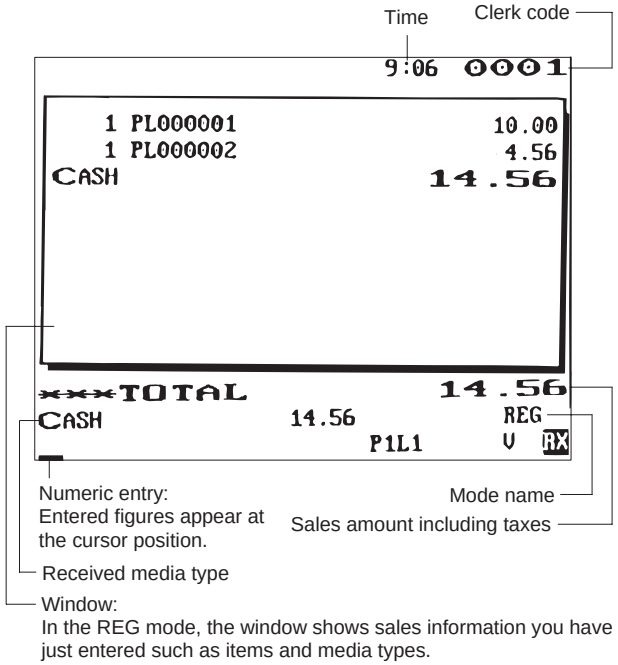
4) Blank key sheet layout



3. Display

1) Operator display

- Screen example 1 (REG mode)



Prive level shift indicator (P1-P7) : Shows the PLU price level currently selected.

PLU level shift indicator (L01-L10) : Shows the PLU level currently selected.

Stock alarm indicator (!) : Appears when the stock of the PLU which you entered is zero or negative.

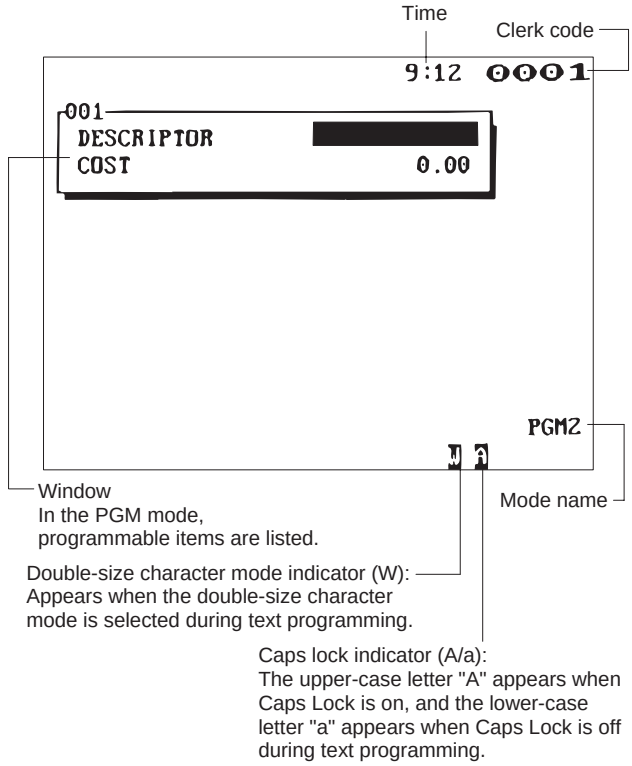
Department shift status indicator (D1-D4) : Shows the department shift status currently selected.

VAT shift status indicator (V) : Appears when the VAT status is shifted.

Receipt ON/OFF status indicator (R) : Appears when the receipt ON-OFF function signs OFF.

Sentinel mark (X) : Appears in the lower right corner of the screen when the cash in drawer exceeds a programmed sentinel amount.
The sentinel check is performed for the total cash in drawer.

- Screen example 2 (PGM mode)


Time
Clerk code
9:12 0001
001
DESCRIPTOR
COST 0.00
PGM2
Window
In the PGM mode, programmable items are listed.
Mode name
Double-size character mode indicator (W):
Appears when the double-size character mode is selected during text programming.
Caps lock indicator (A/a):
The upper-case letter "A" appears when Caps Lock is on, and the lower-case letter "a" appears when Caps Lock is off during text programming.

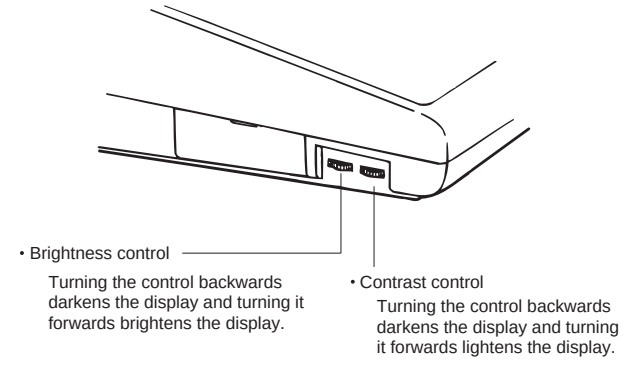
Screen save mode

When you want to save the electric power or save the display's life, use the screen save function. This function can turn the LCD backlight off when any server does not operate the POS terminal for an extended period of time. You can program the time for which your POS terminal should keep the normal status (in which the backlight is "ON") before it goes into the screen save mode.
To go back to the normal mode, press any key.

Device type	LCD display
Dot format	320(W) × 240(H) Full dot
Dot size	0.33 × 0.33 mm
Dot space	0.03 mm
Dot color	White
Back color	Dark blue
Weight	180 g

2) Display adjustment

You can adjust the brightness and contrast of the display by using the corresponding controls.


• Brightness control
Turning the control backwards darkens the display and turning it forwards brightens the display.
• Contrast control
Turning the control backwards darkens the display and turning it forwards lightens the display.

4. Clerk Keys

This POS terminal allows the operator to use the following four clerk identification systems :

- Real clerk keys (standard 6 clerks / max. 126 clerks)
- Clerk code entry (max. 255 clerks)
- Clerk entry keys (max. 10 clerks)
- WMF clerk keys (max. 127 clerks)

The standard POS terminal has been shipped with the real clerk key system being programmed. If you want to change the clerk identification system, contact your authorized SHARP dealer

Real clerk keys (1, 2, 3, 4, 5, and 6)

These keys serve to identify clerks. Put one of the 1 through 6 keys in the clerk switch.

Clerk code entry (1 through 9999)

Enter the clerk code by using the following procedure :

XXXX → [CLERK #] →
Clerk code

Clerk entry keys

[CLK 1] ~ [CLK 10]

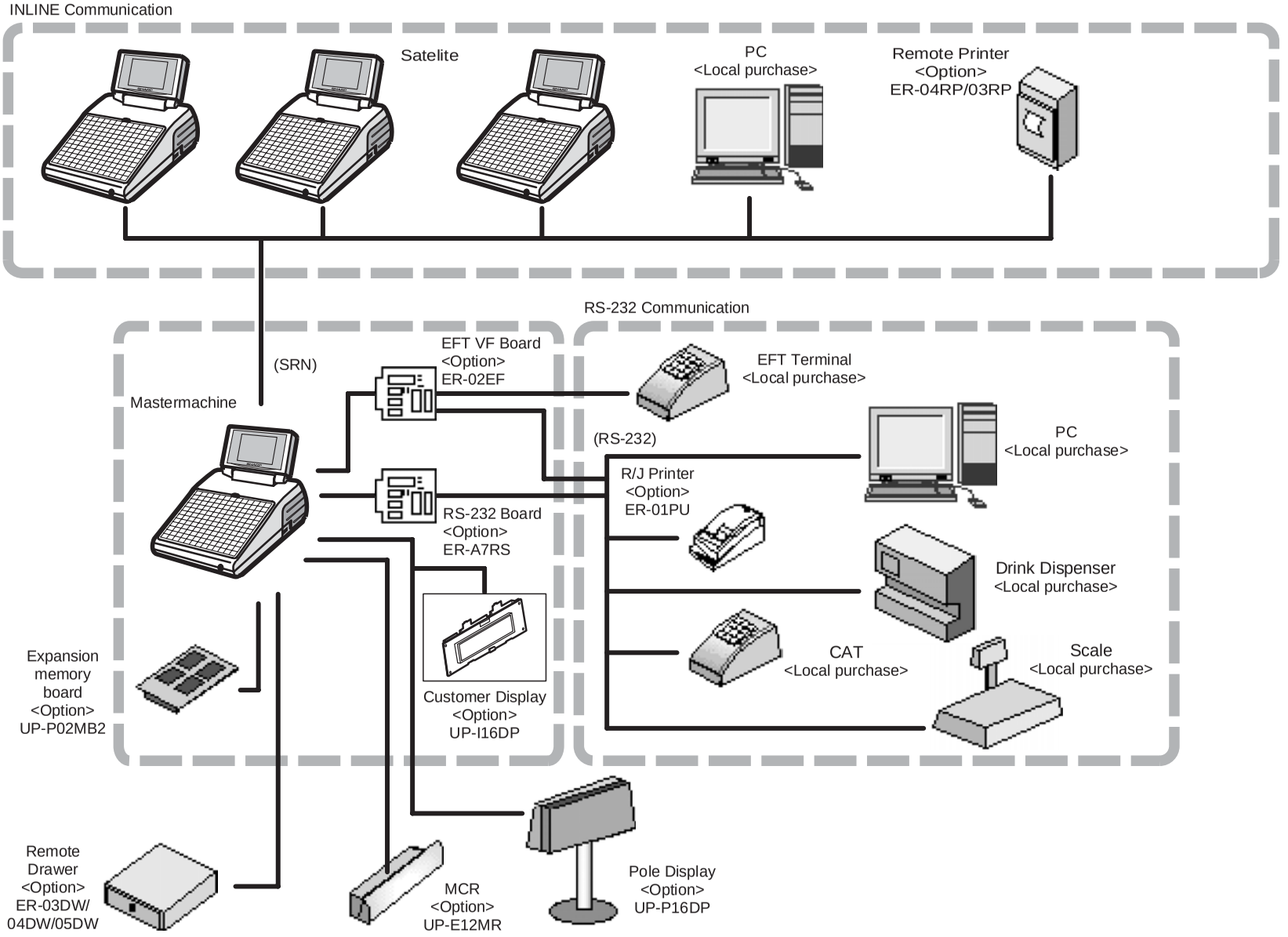
These keys identify clerks. Press any one of these keys.

WMF clerk keys

Put one of the WMF clerk keys in the WMF clerk switch.

CHAPTER 2. OPTIONS

1. System configuration



2. Sales Options

No.	CLASSIFICATION	COMPONENT NAME	MODEL NAME	REMARK
1	Printer	External R/J printer	ER-01PU	Via RS-232 I/F
		Remote printer	ER-03RP	Via SRN I/F
			ER-04RP	
2	Display	Remote display (Pole type)	UP-P16DP	11-Dig. 7-Seg. +16-Dig. Dot
		Customer display	UP-I16DP	11-Dig. 7-Seg. +16-Dig. Dot
3	Drawer	Remote drawer	ER-03DW	
			ER-04DW	
			ER-05DW	
		Coin case	ER-48CC2	4B/8C
			ER-48CC3	4B/8C
			ER-58CC2	5B/8C
		Coin case cover	ER-01CV1-5	
			ER-02CV1-5	
			ER-03CV	
4	Memory	Expansion RAM disk board	UP-P02MB2	2M bytes PS-RAM board
5	On-line function	RS232 I/F board	ER-A7RS	2 ports RS232 I/F
6	OTHER	MCR (Magnetic Card Reader)	UP-E12MR	for ISO 1 & 2 stripe card
		EFT terminal I/F	ER-02EF	

3. Local purchase options

No.	COMPONENT NAME	MODEL NAME	
1	External printer	TM-T85/T88	
		TM-U210	
2	Slip printer	TM-U295	
		TM-H5000	
3	Scale I/F		
4	Drink Dispensor		

4. Service options

No.	NAME	PARTS CODE	DESCRIPTION
1	1 hole clerk key The key No.1 to No.6 ore supplied together with ER-A770.	LKGiM1004BH07	Key No. 7
		LKGiM1004BH08	Key No. 8
		LKGiM1004BH09	Key No. 9
		LKGiM1004BH10	Key No. 10
		LKGiM1004BH11	Key No. 11
		LKGiM1004BH12	Key No. 12
		LKGiM1004BH13	Key No. 13
		LKGiM1004BH14	Key No. 14
		LKGiM1004BH15	Key No. 15
		LKGiM1004BH16	Key No. 16
		LKGiM1004BH17	Key No. 17
		LKGiM1004BH18	Key No. 18
		LKGiM1004BH19	Key No. 19
		LKGiM1004BH20	Key No. 20
		LKGiM1004BH21	Key No. 21
		LKGiM1004BH22	Key No. 22
		LKGiM1004BH23	Key No. 23
		LKGiM1004BH24	Key No. 24
		LKGiM1004BH25	Key No. 25
		LKGiM1004BH26	Key No. 26
		LKGiM1004BH27	Key No. 27
		LKGiM1004BH28	Key No. 28

No.	NAME	PARTS CODE	DESCRIPTION
1	1 hole clerk key The key No.1 to No.6 ore supplied together with ER-A770.	LKGiM1004BH29	Key No. 29
		LKGiM1004BH30	Key No. 30
		LKGiM1004BH31	Key No. 31
		LKGiM1004BH32	Key No. 32
		LKGiM1004BH33	Key No. 33
		LKGiM1004BH34	Key No. 34
		LKGiM1004BH35	Key No. 35
		LKGiM1004BH36	Key No. 36
		LKGiM1004BH37	Key No. 37
		LKGiM1004BH38	Key No. 38
		LKGiM1004BH39	Key No. 39
		LKGiM1004BH40	Key No. 40
		LKGiM1004BH41	Key No. 41
		LKGiM1004BH42	Key No. 42
		LKGiM1004BH43	Key No. 43
		LKGiM1004BH44	Key No. 44
		LKGiM1004BH45	Key No. 45
		LKGiM1004BH46	Key No. 46
		LKGiM1004BH47	Key No. 47
		LKGiM1004BH48	Key No. 48
		LKGiM1004BH49	Key No. 49
		LKGiM1004BH50	Key No. 50
		LKGiM1004BH51	Key No. 51
		LKGiM1004BH52	Key No. 52
		LKGiM1004BH53	Key No. 53
		LKGiM1004BH54	Key No. 54
		LKGiM1004BH55	Key No. 55
		LKGiM1004BH56	Key No. 56
		LKGiM1004BH57	Key No. 57
		LKGiM1004BH58	Key No. 58
		LKGiM1004BH59	Key No. 59
		LKGiM1004BH60	Key No. 60
		LKGiM1004BH61	Key No. 61
		LKGiM1004BH62	Key No. 62
		LKGiM1004BH63	Key No. 63
		LKGiM1004BH64	Key No. 64
		LKGiM1004BH65	Key No. 65
		LKGiM1004BH66	Key No. 66
		LKGiM1004BH67	Key No. 67
		LKGiM1004BH68	Key No. 68
		LKGiM1004BH69	Key No. 69
		LKGiM1004BH70	Key No. 70
		LKGiM1004BH71	Key No. 71
		LKGiM1004BH72	Key No. 72
		LKGiM1004BH73	Key No. 73
		LKGiM1004BH74	Key No. 74
		LKGiM1004BH75	Key No. 75
		LKGiM1004BH76	Key No. 76
		LKGiM1004BH77	Key No. 77
		LKGiM1004BH78	Key No. 78
		LKGiM1004BH79	Key No. 79
		LKGiM1004BH80	Key No. 80
		LKGiM1004BH81	Key No. 81
		LKGiM1004BH82	Key No. 82
		LKGiM1004BH83	Key No. 83
		LKGiM1004BH84	Key No. 84
		LKGiM1004BH85	Key No. 85
		LKGiM1004BH86	Key No. 86
		LKGiM1004BH87	Key No. 87
		LKGiM1004BH88	Key No. 88

No.	NAME	PARTS CODE	DESCRIPTION
1	1 hole clerk key The key No.1 to No.6 ore supplied together with ER-A770.	LKGiM1004BH89	Key No. 89
		LKGiM1004BH90	Key No. 90
		LKGiM1004BH91	Key No. 91
		LKGiM1004BH92	Key No. 92
		LKGiM1004BH93	Key No. 93
		LKGiM1004BH94	Key No. 94
		LKGiM1004BH95	Key No. 95
		LKGiM1004BH96	Key No. 96
		LKGiM1004BH97	Key No. 97
		LKGiM1004BH98	Key No. 98
		LKGiM1004BH99	Key No. 99
		LKGiM1004BH00	Key No. 100
		LKGiM1004BHA1	Key No. 101
		LKGiM1004BHA2	Key No. 102
		LKGiM1004BHA3	Key No. 103
		LKGiM1004BHA4	Key No. 104
		LKGiM1004BHA5	Key No. 105
		LKGiM1004BHA6	Key No. 106
		LKGiM1004BHA7	Key No. 107
		LKGiM1004BHA8	Key No. 108
		LKGiM1004BHA9	Key No. 109
		LKGiM1004BHA0	Key No. 110
		LKGiM1004BHB1	Key No. 111
		LKGiM1004BHB2	Key No. 112
		LKGiM1004BHB3	Key No. 113
		LKGiM1004BHB4	Key No. 114
		LKGiM1004BHB5	Key No. 115
		LKGiM1004BHB6	Key No. 116
		LKGiM1004BHB7	Key No. 117
		LKGiM1004BHB8	Key No. 118
		LKGiM1004BHB9	Key No. 119
		LKGiM1004BHB0	Key No. 120
		LKGiM1004BHC1	Key No. 121
		LKGiM1004BHC2	Key No. 122
		LKGiM1004BHC3	Key No. 123
		LKGiM1004BHC4	Key No. 124
		LKGiM1004BHC5	Key No. 125
		LKGiM1004BHC6	Key No. 126

5. Service tools

No.	NAME	PARTS CODE	PRICE	DESCRIPTION
1	Terminator(50 Ω)	QCNCM7145RCZZ	AZ	for SRN in-line system
2	MCR test card	UKŌG-6718RCZZ	BE	for UP-E12MR
3	RS232 loop back connector	UKŌG-6705RCZZ	BC	for RS232 connector
4	Expansion PWB	CKŌG-6724BHZZ	BX	

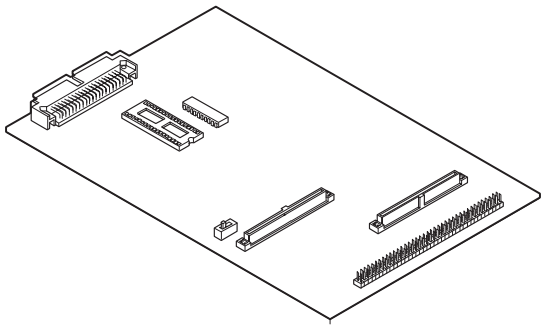
6. Supplies : None

No.	NAME	PARTS CODE	PRICE	
1	Blank key sheet	PSHEK6818BHZZ	AQ	

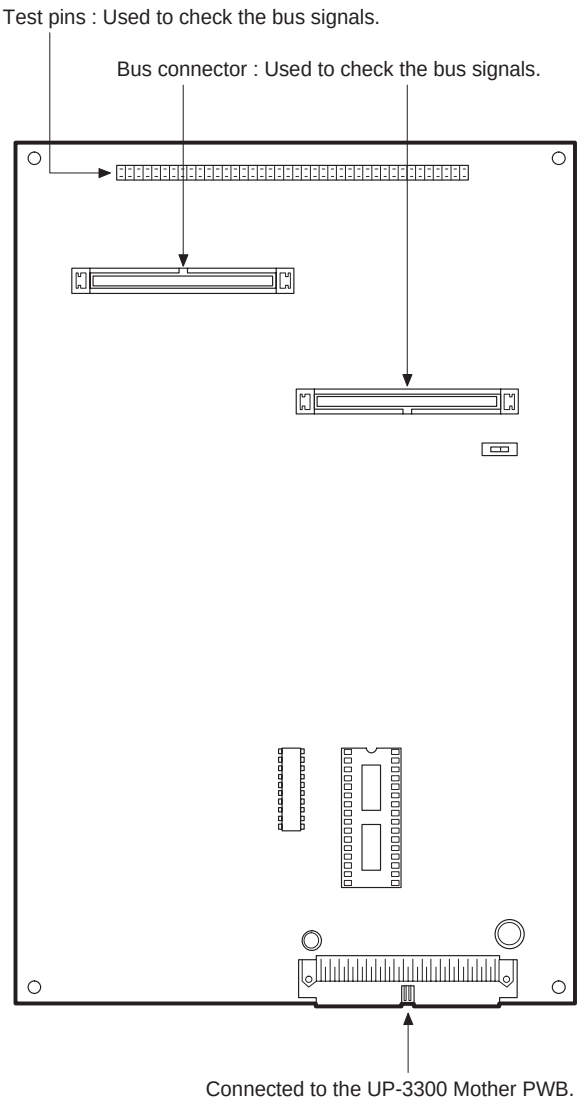
7. How to use service tools

7-1. Expansion PWB : CKOG-6724BHZZ

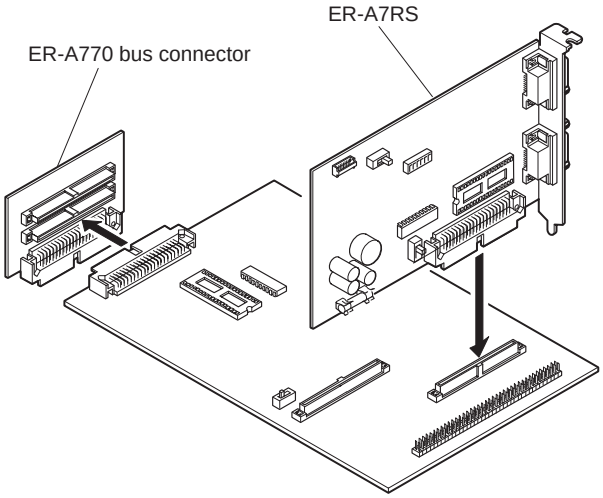
- Extrenal view



- Plain view

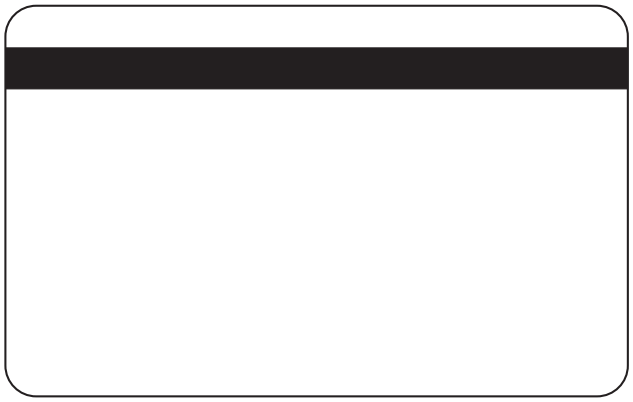


- Connection diagram



7-2. MCR test card: UKOG-6718RCZZ

- Used when executing the diagnostics of the UP-E12MR.
- External view



CHAPTER 3. SERVICE PRECAUTION

1. Adjustment for SRN (IN-LINE) interface circuit

If transistor Q9 in the transmitter/receiver section has been replaced or if the SRN level requires readjustment, the following alignment is required:

1) Tools and Instruments Required

① Oscilloscope (50MHz or better).....1

② ER-A770 1

2) Dummy Network Specifications

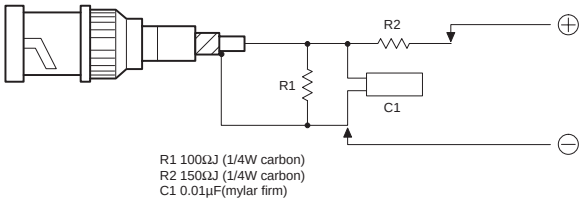


Fig. 1 Dummy network

The oscillator should be connected to the points indicated by ⊕ and ⊖.

⊕ : Connect the positive side of the oscillator.

⊖ : Connect the negative side of the oscillator.

3) Connections

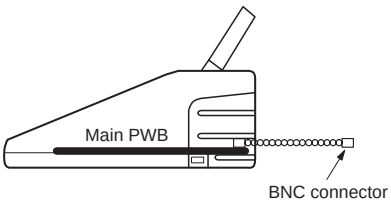


Fig. 2

Attach the BNC connector to the SRN connector (CN7) on the main PWB.

4) Alignment Procedure

① When Using an Oscillator

a) Checking the 1MHz oscillator output

Using an oscilloscope check the 1MHz oscillator's output waveform.

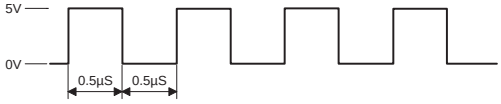


Fig. 3 1MHz oscillator output waveform

NOTE: The oscillator used should have an output impedance of 50Ω.

b) Connecting the oscillator and its adjustment

Connect a dummy network or branch-trunk network to the output of the SRN connector (CN7), and connect the oscillator to the dummy or branch-trunk network.

∗ Waveform adjustment

Adjust VR1 until the signal waveform as shown in Fig. 4 is obtained across TP1 and TP2 (GND).
Turning VR1 clockwise extends the interval of T1.

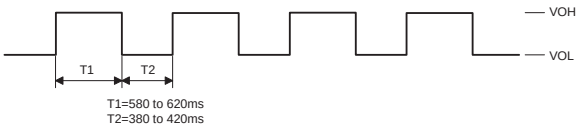


Fig. 4 Receiver regeneration waveform (with dummy network)

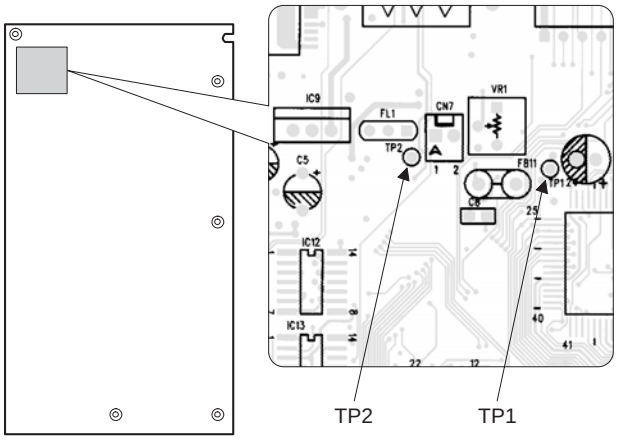


Fig. 5 Board location

2. IPL (Initial program Loading) function

1) Introduction

The application software of the ER-A770 written in the flash ROM.
In the following cases, writing procedure of the application software into the flash ROM is required

- When the flash ROM is replaced with new one. The service part flash ROM does not include the application software in it.
- When IPL writing is required because of change in the software.

∗ The service part ofthe main PWB unit includes the flash ROM with the application software written in it, and there is no need for writing the application software when replacing the main PWB unit.

2) IPL procedure

There are two ways of IPL procedures.

- IPL from P-ROM via ER-A7RS
- IPL from PC communication (Please refer the next section)

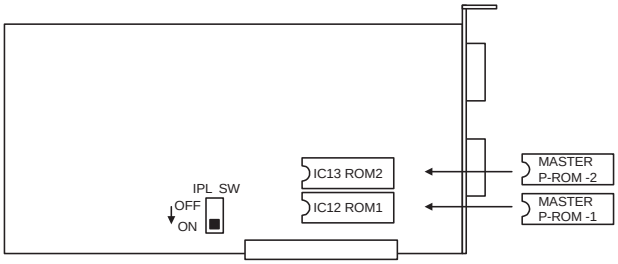
The detailed descriptions on the above procedures are given below.

3) IPL from P-ROM via ER-A7RS

(1) Install the two master ROMs to the IC socket (IC12 , IC13) on the ER-A7RS.

Master ROM -1 : VHI27801RAHxx
Master ROM -2 : VHI27801RAIxx

(2) IPL sitch on the ER-A7RS : Set the IPL SW to ON position.



(3) Install the ER-A7RS to the ER-A770. (The ER-A770 power should be turned OFF.)

(4) Turned on the power of the ER-A770.

(5) The buzzer sounds intermittently during the running of IPL and the program finishes after the buzzer gives five beeps at short intervals.

(6) Turn OFF the power of the ER-A770.

(7) Remove the ER-A7RS from the ER-A770.

(8) Perform the Master reset.

3. ER-A770 Utility tools

1. Outline

This Specification document describes the explanation about "POSUTILITYTOOL.EXEhand "02FD.EXE".

"POSUTILITYTOOL.EXE"and "02FD.EXE" works on Windows 95/98 of PC and they have the following
Functions by connecting ER-A770 with RS232.

POSUTILITYTOOL.EXE	: IPL of ER-A770 Program Object
02FD.EXE	: All RAM Data Upload/Download (PC software tool instead of the current ER-02FD.)

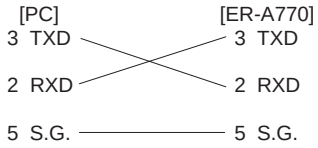
2. Environment

PC and ER-A770 are connected by RS232.

Connect the CH2 port of the ER-A770 to the RS-232 interface of the PC.

Fig. 1 Connection between PC and ER-A770

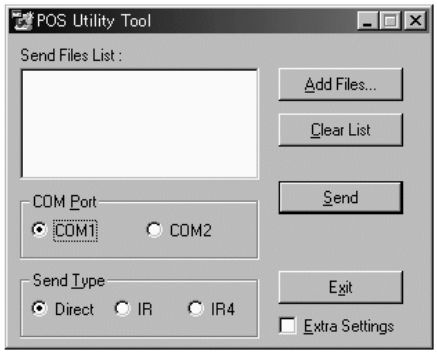
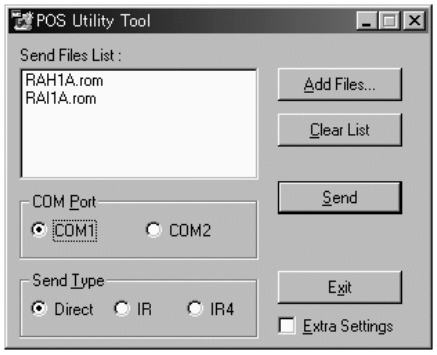
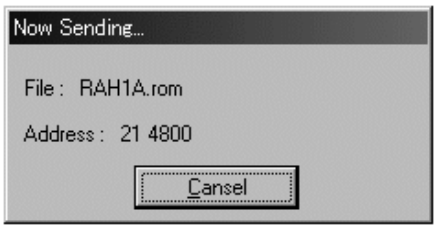
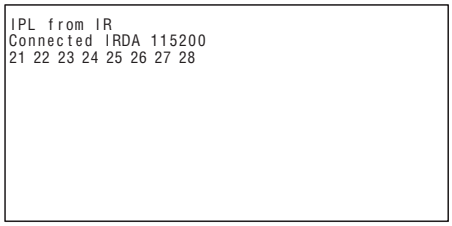
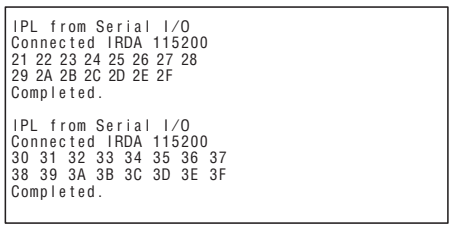
RS232 Cable Connecting:



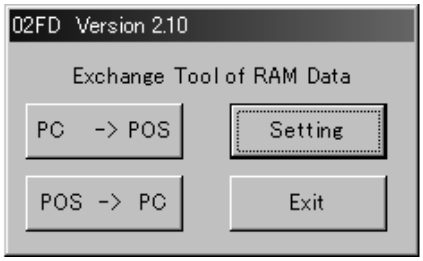
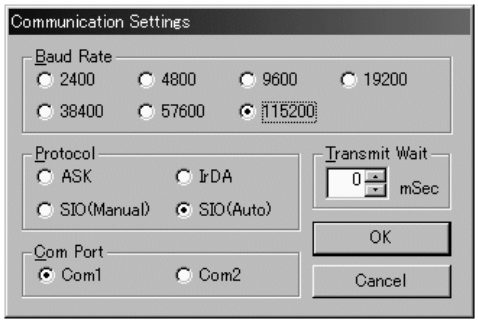
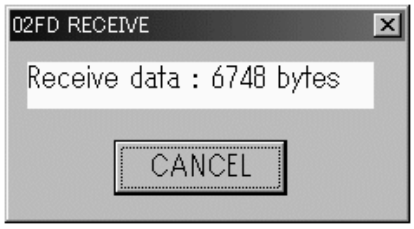
3. Procedure

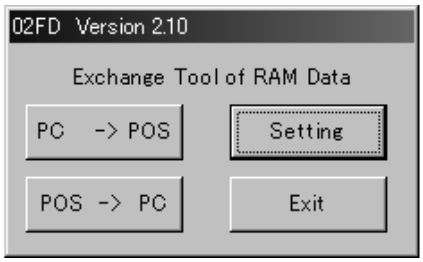
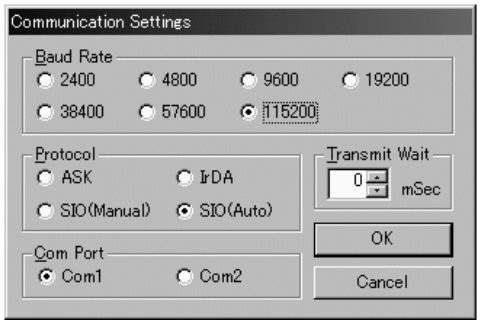
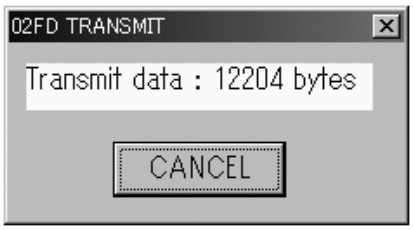
3.1 POS UTILITY TOOL

No	Procedure on P.C. side	No	Procedure on ER-A770 side
1	Install "POSUTILITYTOOL.EXE" on the P.C.		
		2	Turn OFF the power.
		3	Select "IPL Mode". Set "IPL Switch" of ER-A770 to "ON". IPL SW OFF ON
		4	Turn ON the power.
		5	Starting of "IPL Mode". ER-A770 shows "IPL from Serial I/O" IPL from Serial I/O
6	Connect P.C. and ER-A770 (CH2) via RS232. (Fig 1)		

No	Procedure on P.C. side	No	Procedure on ER-A770 side
7	Execute "POSUTILITUTOOL.EXE" on P.C. *Don't execute the other Software at the same time. 		
8	Select the ROM object Files by "Add Files.." button. 		
9	Push "SEND" button. Program data is sent to ER-A770 automatically. 	9	Program data is received from P.C. automatically. ER-A770 shows 
10	When sending is completed, the initial Window is shown after "Complete" window.	10	ER-A770 shows "Completed." 
		11	Turn OFF the power.
		12	Select "Normal Mode". Set "IPL switch" to "OFF". (Ref. Hardware manual)
		13	Execute "Service Reset" on ER-A770.

3.2 02FD

No	Procedure on P.C. side	No	Procedure on ER-A770 side
1	Install "02FD.EXE" on the P.C. ALL RAM Data UpLoad : Go to "2" ALL RAM Data DownLoad : Go to "9"		
2	ALL RAM Data UpLoad Connect P.C. and ER-A770 (CH2) via RS232. (Fig 1)	2	Enter the SRV mode. Select " 2 SETTING ". Select " 14 BACKUP SEND"
		3	ER-A770 shows BACKUP SEND SEND DATA ALL RAM SPEED PROGRAMMED SPEED
4	Execute "02FD.EXE" on P.C. *Don't execute the other Software at the same time. 		
5	Set the Communication method by "Setting" Button.  Push "OK" Button.		
6	Push "Receive Start" Button. And Select the Receiving File.		
7	Communication starts. 	7	Push TL key. ER-A770 shows SENDING 00000
8	UpLoad is completed. The initial Window is shown. Push "Exit" Button.	8	UpLoad is completed. The SETTING menu is shown.
9	ALL RAM Data UpLoad Connect P.C. and ER-A770 (CH2) via RS232. (Fig 1)	9	Enter the SRV mode. Select " 2 SETTING". Select " 15 BACKUP RECEIVE"
		10	ER-A770 shows BACKUP RECEIVE SPEED PROGRAMMED SPEED Push TL key.

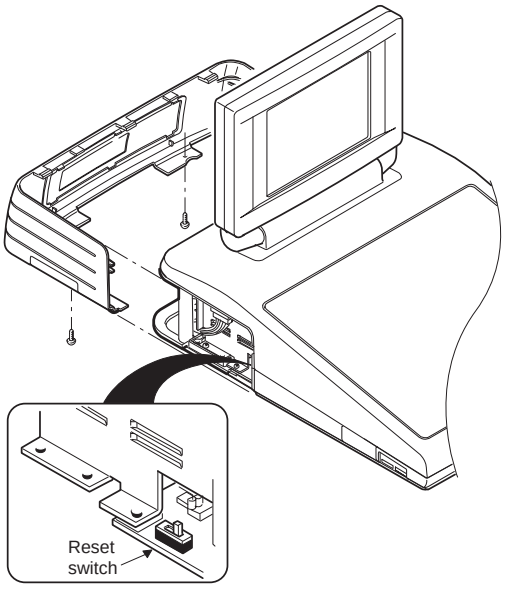
No	Procedure on P.C. side	No	Procedure on ER-A770 side
11	Execute "02FD.EXE" on P.C. *Don't execute the other Software at the same time. 		
12	Set the Communication method by "Setting" Button.  Push "OK" Button.		
13	Push "Transmit Start" Button. And Select the Sending File.		
14	Communication starts. 	14	ER-A770 shows
15	DownLoad is completed. The initial Window is shown. Push "Exit" Button.	15	DownLoad is completed. The SETTING menu is shown.

4. Note for handling of LCD

- The LCD elements are made of glass. BE careful not to give them strong mechanical shock, or they may be broken. Use extreme care not to break them.
- If the LCD element is broken and the liquid is leaked, do not lick it. If the liquid is attached to your skin or cloth, immediately clean with soap.
- Use the unit under the rated conditions to prevent against damage.
- Be careful not to drop water or other liquid on the display surface.
- The reflection plate and the polarizing plate are easily scratched. BE careful not to touch them with a hard thing such as glass, tweezers. Never hit, push, or rub the surface with hard things.
- When installing the unit, be careful not to apply stress to the LCD module. If an excessive stress is applied, abnormal display or uneven color may result.

CHAPTER4. SRV RESET (Program Loop Reset) and switch to SRV mode

In the ER-A770, the following reset switch (location No. : SW1) is used to switch to the service (SRV) mode and to reset.

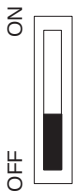


RESET SW

SW1

Rear side :"ON" position(Reset state)

RESET SW



Front side :"OFF" position(Run state)

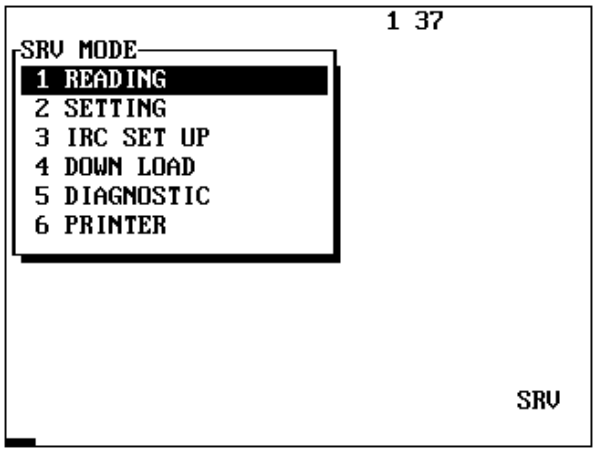
SRV. reset

Used to return the machine back to its operation state after a lock up has occurred.

PROCEDURE

1) Turn off the AC switch.
2) Set the reset switch to "ON" position
3) Turn on the AC switch. (Wait one second)
4) Turn to "OFF" the reset switch.
5) The SRV mode is displayed as shown below.

   DISPLAY:



CHAPTER 5. MASTER RESET (All Memory Clear)

There are two possible methods to perform a master reset.

MRS-1 (Master resetting 1)

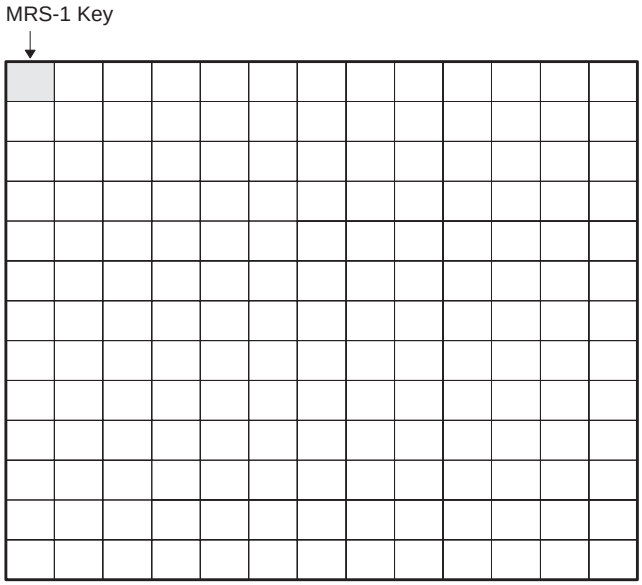
Used to clear all memory contents and return machine back to its initial settings.

Return keyboard back to default for default kyeboard layout.

PROCEDURE

1) Turn off the AC switch.
2) Set the reset switch to "ON" position
3) Turn on the AC switch. (Wait one second)
4) While holding down MRS-1 key , turn to "OFF" the reset switch.

   ∗ MRS-1 key : The key located on Left upper corner of the key-board.



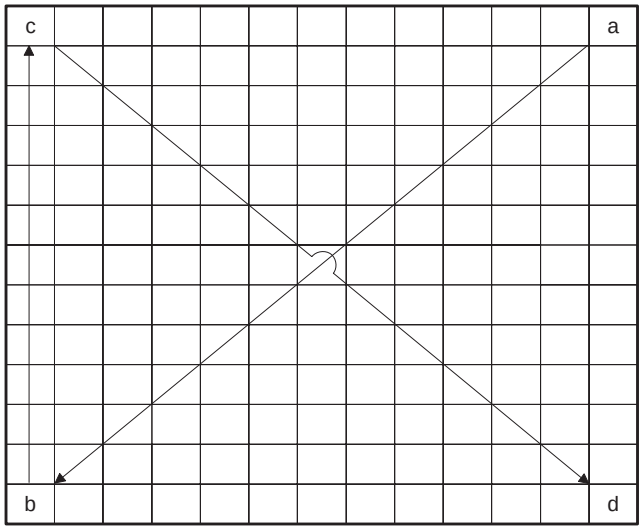
keyboard layout

5) Enter the password key operation

   DISPLAY:

   ENTER PASSWOPRD

   Password input procedure: Press the four corners of the key-board in the sequence of a, b, c, and d.



keyboard layout

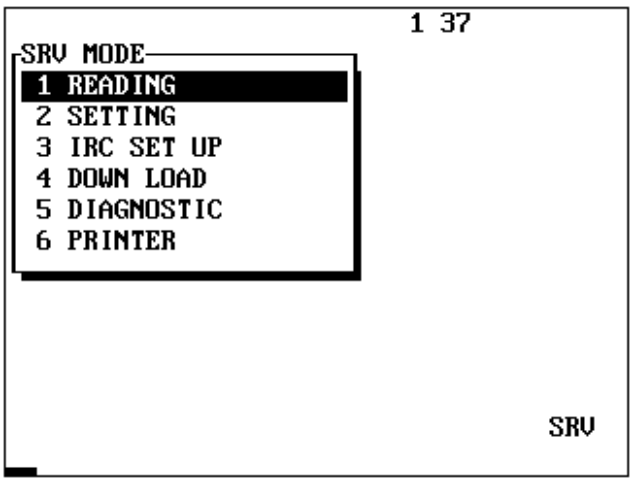
6) Master reset is started.

   DISPLAY:

   MASTER RESET

7) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

   DISPLAY:



MRS-2 (Master resetting 2)

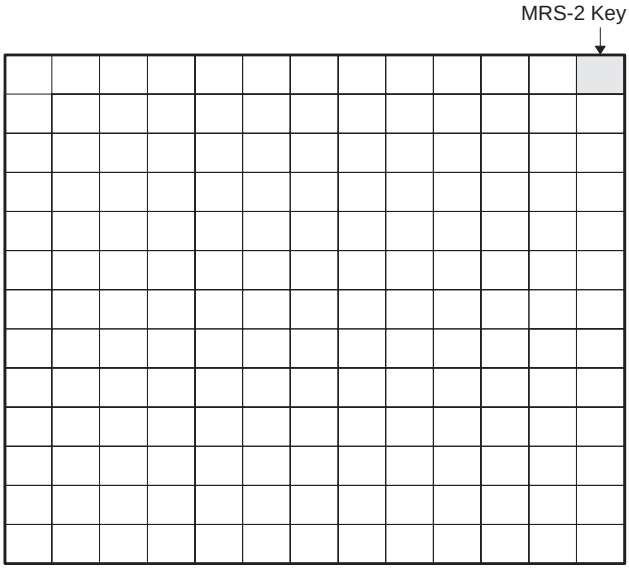
Used to clear all memory and keyboard contents. This reset returns all programming back to defaults.

The keyboard must be entered by hand. This reset is used if an application needs different keyboard layout other than that supplied by a normal MRS-1.

PROCEDURE

1) Turn off the AC switch.
2) Set the reset switch to "ON" position
3) Turn on the AC switch. (Wait one second)
4) While holding down MRS-2 key , turn to "OFF" the reset switch.

   ∗ MRS-2 key: The key located on Right upper corner of the keyboard.



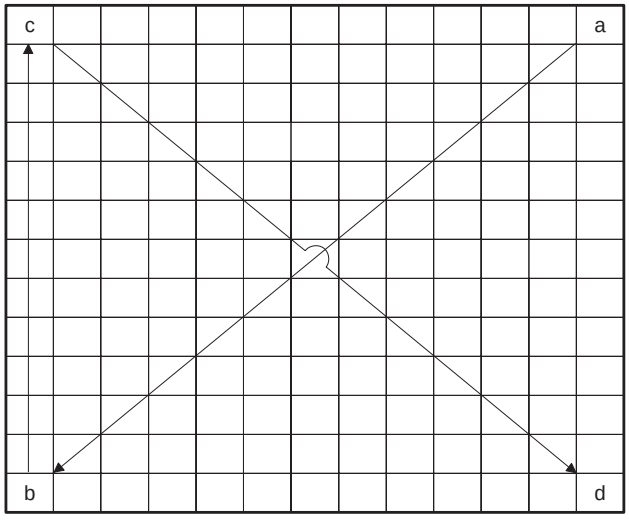
keyboard layout

5) Enter the password key operation

   DISPLAY:

   ENTER PASSWOPRD

   Password input procedure: Press the four corners of the key-board in the sequence of a, b, c, and d.



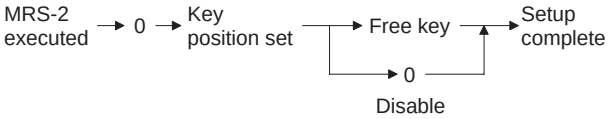
keyboard layout

6) Set the fixed keys in the table below. (Start from the zero "0" key, The keys are displayed sequentially.)

   DISPLAY:

   ENTER 0 KEY

   [Key setup procedure]



   NOTES:

   ∗ 1: When the 0 key is pressed, the key of the key number on display is disabled.

   ∗ 2: Push the key on the position to be assigned. With this, the key of the key number on display is assigned to that key position.

   ∗ 3: When relocating the keyboard, the PGM 1/2 mode use standard key layout.

Key No.	Key name	Key No.	Key name	Key No.	Key name
001	"0" key	011	"00" key	021	RIGHT "→" key
002	"1" key	012	"000" key	022	"CANCEL" key
003	"2" key	013	Decimal point "•" key	023	"ENTER" key
004	"3" key	014	"CL" key	024	"TL" key
005	"4" key	015	"⊘" key		
006	"5" key	016	"SBTL" key		
007	"6" key	017	"MODE" key		
008	"7" key	018	UP "↑" key		
009	"8" key	019	DOWN "↓" key		
010	"9" key	020	LEFT "←" key		

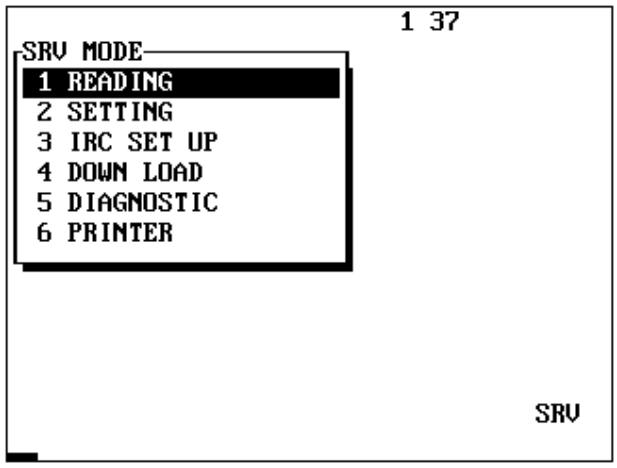
7) Master reset is started.

   DISPLAY:

   MASTER RESET

8) After completion of the master reset, the buzzer sounds three times and the following SRV mode display is shown.

   DISPLAY:



CHAPTER 6. DIAGNOSTICS SPECIFICATIONS

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1) Magnetic Card Reader Check 10
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1) Drawer 1 Check 10
2) Drawer 2 Check 10

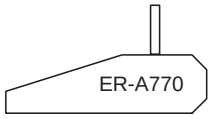
1. General

This diagnostics program is used for simplified check of the ER-A770 series operations in servicing.
The diagnostics program is built in the standard ROM.

2. System configuration

2-1. Test system

ER-A770 only



3. Diagnostics

Starting the diagnostics

This diagnostics program is written in the external ROM and executed by the CPU (H8/510). To operate this program, the following conditions must be satisfied.

① The power for the logic system is proper.
(+5V, VRAM, VCKDC, POFF, +20V)
② The input/output pins and the internal logic of the CPU are normal. In addition, CKDC9, MPCA8, the system bus, and the standard ROM/RAM are normal.

To start the machine for the first time, perform the master reset.

In order to add an option unit when the machine is normally operating, perform the program reset.

1) Master reset procedure

① Turn off the power.
② Set the CKDC reset switch to RESET position.
③ Turn on the power.
④ While pressing the specified key, set the CKDC reset switch to the normal position.

2) Program reset (service reset) procedure

① Turn off the power.
② Set the CKDC reset switch to RESET position.
③ Turn on the power.
④ Set the CKDC reset switch to the normal position. (Do not press any key.)

3-1. Execution of diagnostics

To start the diagnostics, select "DIAGNOSTICS" with the cursor in the menu selection in SRV mode, and press the enter key.
The DIAG MAIN MENU is started and the following menu screen is display. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the individual diagnostics program is completed, the display returns to the menu screen. To terminate the diagnostics, press the CANCEL key. Then the display returns to the SRV mode menu screen.

```
ER-A770 Diagnostics V 1.0A

  Product & Test Diagnostics
  RAM Diagnostics
  ROM & SSP Diagnostics
  Clock & Keyboard & Clerk Diagnostics
  Serial I/O Diagnostics
  LCD Diagnostics
  Rear & Pole Display Diagnostics
  SRN Diagnostics
  EFT Diagnostics
  MCR Diagnostics
  Drawer Diagnostics
  Diagnostics End
```

"Product & Test Diagnostics" is used only in the production process, and must be not used in servicing.

3-2. RAM Diagnostics

This diagnostics is used to test the standard RAM and the expansion RAM.

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed.

```
RAM Diagnostics

  Standard RAM Check
  UP-P02MB2 Check
```

1) Standard RAM Check

① Check content

For the pseudo SRAM of the standard RAM 1MB, the following check is performed. The memory contents will not be changed by this check.

The following processes are performed for the memory address (700000H ~ 7FFFFFH) to be checked.

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated.

Check point address = 700000H, 700001H
700002H, 700004H
700008H, 700010H
700020H, 700040H
700080H, 700100H
700200H, 700400H
700800H, 701000H
702000H, 704000H
708000H, 710000H
720000H, 740000H
780000H

② Display

The screen displays the capacity of RAM in the unit of 64 KB.

```
Standard RAM Check

 Standard memory size : 1024KB PASS!!(or ERROR!!)

 Error Address xxxxxxH
     Write Data xxxxH
      Read Data xxxxH
```

The error address and the bit are displayed only when the error occurs. (If the error does not occur, they are not displayed.)

③ Terminating procedure

After completion of check, press the CANCEL key.

2) UP-P02MB2 Check

① Check content

The UP-P02MB2 presence check is performed in the following procedure. The memory contents must not be changed by this check.

- 55AAH is written into 9FFFFEH.
- 9FFFFEH is read and compared with 55AAH. If the both data are correct, the following procedure is performed. The system reads 9FFFFEH and compares it with 55AAH. If both data are correct, the following tests will be performed. If not, the screen displays the message "Extended RAM size : 0KB", and ends the test.

For the UP-P02MB2, the following check is performed.

The following processes are performed for the check address (800000H ~ 9FFFFFH).

PASS1: Memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read/compare, data "5555H" write

PASS4: Data "5555H" read/compare, data "AAAAH" write

PASS5: Data "AAAAH" read/compare

PASS6: Memory data writed the saved data

In case of a compare error in the check sequences of PASS1 ~ PASS6, an error display is made. If there is no error at all, the check is normally terminated.

In addition, the following address check is performed in the above check sequence.

In case of an error, an error display is made and read/write of the address where the error occurred is repeated without performing the check.

Check point address = 800000H,800001H
800002H,800004H
800008H,800010H
800020H,800040H
800080H,800100H
800200H,800400H
800800H,801000H
802000H,804000H
808000H,810000H
820000H,840000H
880000H,900000H

② Display

The screen displays the capacity of RAM in the unit of 64 KB.

```
UP-P02MB2 Check

  Extended RAM size : 2048KB PASS!!(or ERROR!!)

  Error Address xxxxxxH
      Write Data xxxxH
       Read Data xxxxH
```

The error address and the bit are displayed only when the error occurs. (If the error does not occur, they are not displayed.)

③ Terminating procedure

After completion of check, press the CANCEL key.

3-3. ROM & SSP Diagnostics

The standard ROM and the service ROM are checked. The SSP circuit is also checked.

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed.

```
ROM & SSP Check

   Standard ROM Check
   Service ROM Check
   SSP Check
```

1) Standard ROM Check

① Check contents

The standard ROM area (200000H ~ 3FFFFFH) is added in the unit of byte. If the lower two digits of the result is 20H, it is normal. The ROM version and the model name code which are stored in address 31FFE0H ~ 31FFEFH where the ROM version and the check sum correction data are stored are displayed. The format of data (ASCII) to be stored is as follows:

31FFE0H ~ 31FFEFH: Model name code (example: ER-A770. Display is made up to 00H of data.)

31FFF0H ~ 31FFF9H: 27801R****(****=PROGRAM VERSION)

31FFFAH ~ 31FFFBH: BLOCK NO. ("20" ~ "3F")

31FFFCH: TERMINATOR ("=")

31FFFDH ~ 31FFFEH: BLOCK VERSION (example "00")

31FFFFH: CHECK SUM CORRECTION DATA

The flash ROM used as the standard ROM has rewriting block of 64KB as the unit. To control the version in each block, the composition is the same as the above 31FFF0H or later and arranged in each 64KByte. At that time, correction is made so that the sum of each block becomes 01H, and the total of 2MByte is 20H.

The program version of the IPL is displayed so that 0PAGE (BLOCK) where the IPL is stored is individually controlled.

② Display

The screen displays the capacity of RAM in the unit of 64 KB.

```
Standard ROM Sum Check : PASS!!(or ERROR!!)
IPL PROGRAM Version
                **
APL PROGRAM Version          ← Displays the version.
        27801R**** ER-A770
        27801R**** ER-A770
BLOCK Version
 20=**,21=**,22=**,23=**,24=**,25=**,26=**,27=**
 28=**,29=**,2A=**,2B=**,2C=**,2D=**,2E=**,2F=**
                     :
```

③ Terminating procedure

After displaying the check result, press the CANCEL key to terminate the check.

2) SERVICE ROM Check

① Check content

For the SERVICE ROM area (D00000H ~ EFFFFFH) consisting of two EPROMs, addition is made in the unit of byte for each chip. The lower two digits of the result are 10H, it is regarded as normal.

The ROM version and the model name code which are stored in address D1FFE0H ~ D1FFFFH where the ROM version and the check sum correction data are stored are displayed. The format of data (ASCII) to be stored is as follows:

D1FFE0H ~ D1FFEFH: Model name code (example: ER-A770. Display is made up to 00H of data.)

D1FFF0H ~ D1FFF9H: 27801R****(****=PROGRAM VERSION)

D1FFFAH ~ D1FFFBH: BLOCK NO. ("20" ~ "2F")

D1FFFCH: TERMINATOR ("=")

D1FFFDH ~ D1FFFEH: BLOCK VERSION (example "00")

D1FFFFH: CHECK SUM CORRECTION DATA

This SERVICE ROM allows to write into the FLASH ROM when re-execution is impossible because of an abnormality during re-writing into the FLASH ROM. The composition is the same as the standard ROM.

The program version of the IPL is displayed so that 0PAGE (BLOCK) where the IPL is stored is individually controlled.

② Display

The screen displays the capacity of RAM in the unit of 64 KB.

```
Standard ROM Sum Check : PASS!!(or ERROR!!)
IPL PROGRAM Version
                **
APL PROGRAM Version          ← Displays the version.
        27801R**** ER-A770
        27801R**** ER-A770
BLOCK Version
 20=**,21=**,22=**,23=**,24=**,25=**,26=**,27=**
 28=**,29=**,2A=**,2B=**,2C=**,2D=**,2E=**,2F=**
                     :
```

③ Terminating procedure

After displaying the check result, press the CANCEL key to terminate the check.

3) SSP Check

① Check content

By starting this check program, the SSP setting for checking is automatically performed and the SSP check is executed and the result is displayed.

The SSP check sets data for check in the vacant space in the SSP entry register, and deletes the data for check after completion of checking. Therefore, the already set data are not changed by this check.

② Display

```
SSP Check

  SSP (NMI) Check       : PASS!!(ERROR!!)
```

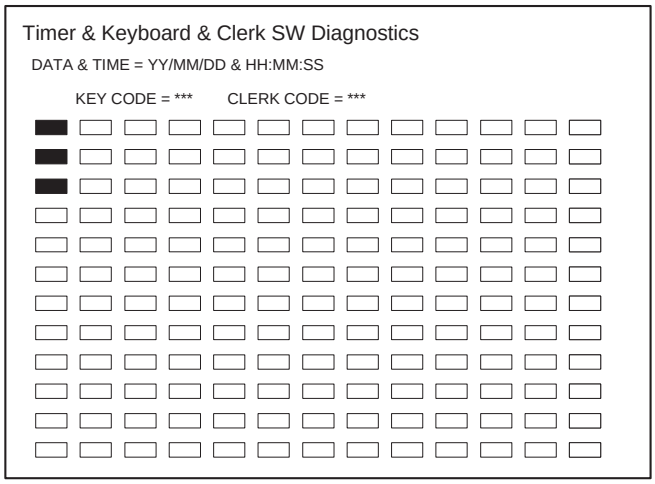
③ Terminating procedure

After displaying the check result, press the CANCEL key to terminate the check.

3-4. Timer & Keyboard & Clerk Switch Diagnostics

The operation of the clock crystal of CKDC, the keyboard, and the clerk switch are tested.

When the CANCEL key is pressed, the display returns to the diagnos tics menu.



1) Timer Check

① Check content

The operation of the clock crystal of CKDC9 is checked.

The screen displays "YY/MM/DD & MM:HH:SS". Make sure that the time displayed is updated.

2) Keyboard Check

① Check content

The A770 main body keyboard input test is performed. The position code corresponding to the inputted key is displayed in three digits. The key layout corresponding to the input is displayed on the LCD screen. Press the corresponding key to input. The display of the inputted key is changed from white square □ to black square ■ and a catch sound is generated.

3) Clerk SW Check

① Check content

The code of the key which is inserted into the clerk key switch is displayed in a decimal number.

3-5. RS232 I/F Diagnostics

The main PWB and the option PWB (RS232 interface of ER-A7RS) are checked. Attach the 9-pin D-Sub loop back connector (UKOG-6717RCZZ) of wiring in Fig. 3-11.

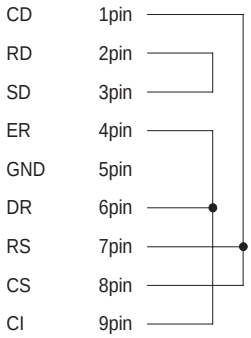


Fig. 3-11. Wiring diagram of loop back connector (UKOG-6717RCZZ)

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the CANCEL key is pressed, the display returns to the diagnostics menu.

When setting channels of RS232, do not set two or more ports to one channel. In the ER-A770, max. two units of ER-A7RS can be installed. In each PWB, do not set two or more ports to the same channel. If two or more ports should be set to one channel, the hardware would be destroyed.

```
RS232 I/F Diagnostics

  CHANNEL Check
  CH1 Check
  CH2 Check
  CH3 Check
  CH4 Check
  CH5 Check
  CH6 Check
  CH7 Check
  CH8 Check
```

1) CHANNEL Check

① Check content

The CHANNEL setting of the connected RS232 is displayed. The display content and the setting of DIP SW for CHANNEL setting on the RS232 I/F PWB are compared.

Since the RS232 on the main PWB of the ER-A770 is fixed to CH1 and CH8, that in the ER-A7RS must be set to CH2 ~ CH7.

Relationship between the physical channel and logical channel of the ER-A770's RS232.

The ER-A770 comes equipped with 2 channels of the RS232C interface as standard.

These two channels are expressed as physical channels "CH1" and "CH2" on the cabinet and application. On hardware, however, the "CH2" is defined as a logical channel "CH8" because it has a different circuit configuration.

Therefore, the relationship of channel definitions between the cabinet indication and the RS232 I/F Diag is as shown in the table below.

Cabinet indication	Logical channel	Definition in Diag.	Application
CH1	CH1	CH1	CH1
CH2	CH8	CH8	CH2

```
RS232 I/F Diagnostics

   CHANNEL Check
   CH1 = exist!        ← Display when channel present
   CH2 = exist!
   CH3 = none!         ← Display when no channel
   CH4 = none!
   CH5 = none!
   CH6 = none!
   CH7 = none!
```

(Reference) ER-A7RS CHANNEL setting (In the table below, "1" = SW OFF, "0" = SW ON.)

ER-A7RS CON3

S1-1	S1-2	S1-3	LOGICAL CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Impossible to set
0	1	0	CHANNEL 2:
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6
1	1	1	CHANNEL 7

ER-A7RS CON3

S1-4	S1-5	S1-6	LOGICAL CHANNEL
0	0	0	Invalid
0	0	1	CHANNEL 1: Impossible to set
0	1	0	CHANNEL 2
0	1	1	CHANNEL 3
1	0	0	CHANNEL 4
1	0	1	CHANNEL 5
1	1	0	CHANNEL 6
1	1	1	CHANNEL 7

② Terminating procedure

Press the CANCEL key to terminate the check.

2) CH1 Check

① Check content

When the channel is not set, an error display is made (ERROR:CH1). When the channel is set, the following check is performed.

- Control signal check

ERn	RSn	DRn	CIn	CDn	CSn
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check of the above inputs and the interruption check of CS, CI, and CD are performed.

In the read check, ER and RS are changed over in the above sequence and the logic states of DR, CI, CD, and CS are checked.

If the logic differs from that in the table, an error display is made.

"ON" in the table means Active LOW, and "OFF" means Active HIGH.

In the interruption check, an interruption of CS, CI, or CD is allowed one by one. (MASK is canceled.)

If an interruption is not made when each signal is active, or if an interruption is made when each signal is not active, an error display is made.

The above check is repeated four cycles.

- Data transfer check
  The loop back data (256 bytes) of 00H ~ 0FFH are used for data transfer check. The baud rate is set to 38400BPS.
- Timer check (RS232 on board timer)
  Before performing the check, set the timer to RCVDT start and 5ms. Then perform the following procedure.

  ∗ During execution of the check, TRQ- must not be generated.

  ∗ After 5ms from completion of the check, TRQ- must be generated.

② Display

```
RS232 CH1 Check

ER-DR          :      ERROR!!
```

All the contents of an error must be displayed.

ERROR No.	ERROR display	ERROR content
1	ER-DR:ERROR	ER-DR LOOP ERROR
2	ER-CI:ERROR	ER-CI LOOP ERROR
3	RS-CD:ERROR	RS-CD LOOP ERROR
4	RS-CS:ERROR	RS-CS LOOP ERROR
5	CI INT:ERROR	CI interruption is not made.
6	CD INT:ERROR	CD interruption is not made.
7	CS INT:ERROR	CS interruption is not made.
8	TXEMP:ERROR	TXEMP is not set.
9	TXEMP INT:ERROR	TXEMP interruption is not made.
10	TXRDY:ERROR	TXRDY interruption is not made.
11	TXRDY INT:ERROR	TXRDY interruption is not made.
12	RCVRDY:ERROR	RCVRDY is not set. (Reception enabled. TR-Q is generated during check)
13	RCVRDY INT:ERROR	RCVRDY interruption is not made.
14	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR)
15	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR
16	TIMER:ERROR	TIMER ERROR (TMRQ is not set after completion of check.)
17	TIMER INT:ERROR	TRQ-1 interruption is not made.

③ Terminating procedure

Press the CANCEL key to terminate the check.

3) CH2 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

4) CH3 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

5) CH4 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

6) CH5 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

7) CH6 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

8) CH7 Check

① Check content

The check procedure, the display, and the terminating procedure are the same as CH1 Check.

9) CH8 Check

① Check content

When the channel is set, the following check is performed.

- Control signal check

Ern	RSn	DRn	Cin	CDn	CSn
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

The read check of the above inputs.

In the read check, ER and RS are changed over in the above sequence and the logic states of DR, CI, CD, and CS are checked.

If the logic differs from that in the table, an error display is made.

"ON" in the table means Active LOW, and "OFF" means Active HIGH.

The above check is repeated four cycles.

- Data transfer check
  The loop back data (256 bytes) of 00H ~ 0FFH are used for data transfer check. The baud rate is set to 115200BPS.

② Display

```
RS232 CH1 Check

ER-DR          :      ERROR!!
```

All the contents of an error must be displayed.

ERROR No.	ERROR display	ERROR content
1	ER-DR:ERROR	ER-DR LOOP ERROR
2	ER-CI:ERROR	ER-CI LOOP ERROR
3	RS-CD:ERROR	RS-CD LOOP ERROR
4	RS-CS:ERROR	RS-CS LOOP ERROR
5		
6		
7		
8	TXEMP:ERROR	TXEMP is not set.
9	TXEMP INT:ERROR	TXEMP interruption is not made.
10	TXRDY:ERROR	TXRDY interruption is not made.
11	TXRDY INT:ERROR	TXRDY interruption is not made.
12	RCVRDY:ERROR	RCVRDY is not set. (Reception enabled. TR-Q is generated during check)
13	RCVRDY INT:ERROR	RCVRDY interruption is not made.
14	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR)
15	SD-RD:ERROR	SD-RD LOOP ERROR (DATA ERROR, FRAMING ERROR, etc.)
16		
17		

③ Terminating procedure

Press the CANCEL key to terminate the check.

3-6. Liquid Crystal Display Diagnostics

The ER-A770 LCD display is checked.

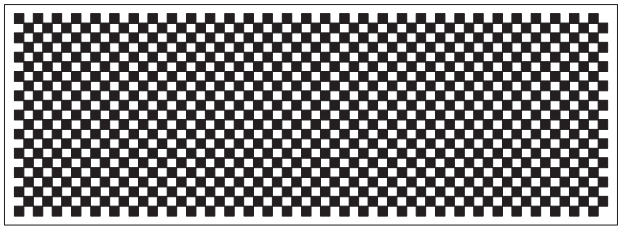
The test program displays the patterns in the following sequence. Every time when the ENTER key is pressed, the next pattern is displayed. When the ENTER key is pressed at the final pattern, or when the CANCEL key is pressed at the midst of the check, the display returns to the menu screen.

1) Liquid Crystal Display Check

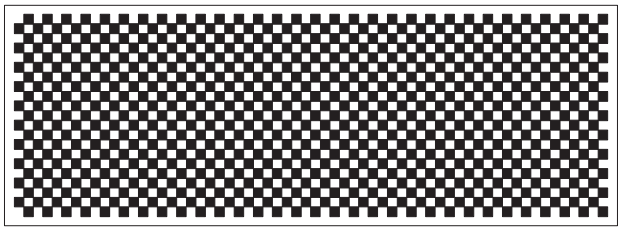
① Check content

The test patterns are displayed in the following sequence. When the ENTER key is pressed, the next pattern is displayed.

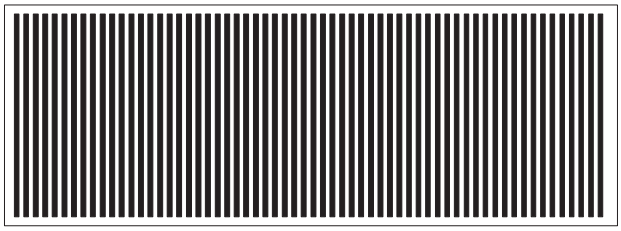
- Black and white pattern at 1 dot pitch



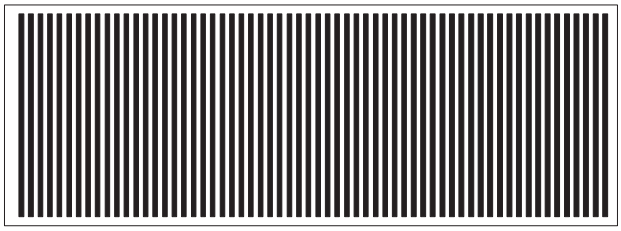
- Reversed pattern of the above



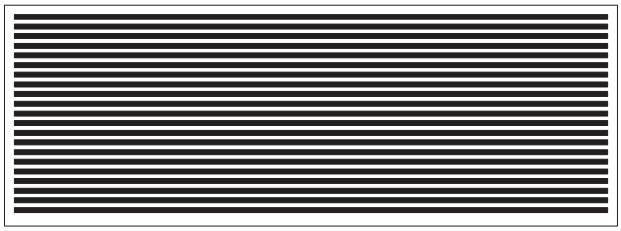
- Vertical stripe pattern at 1 dot pitch



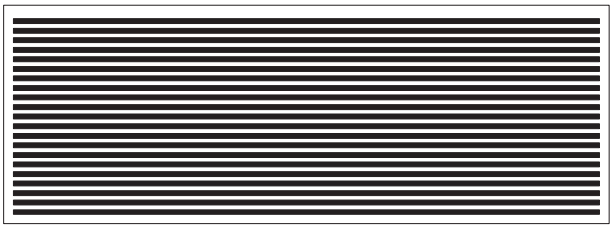
- Reversed pattern of the above



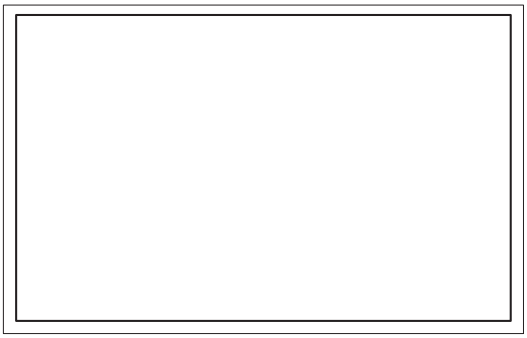
- Horizontal stripe pattern at 1 dot pitch



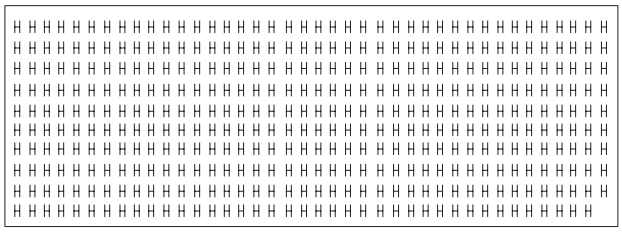
- Reversed pattern of the above



- The outermost peripheral of the LCD's active area is displayed in one-dot line.



- "H" pattern. "H" is displayed in 40 digits and 15 lines. The 15th line only has 39 digits of "H."



② Terminating procedure

Press the ENTER key at the final pattern, or press the CANCEL key to terminate the check.

3-7. Rear & Pole Display Diagnostics

The rear display is checked.

The test program displays the following patterns. When the CANCEL key is pressed, the display returns to the diagnostics menu.

1) Rear & Pole Display Check

① Check content

The test patterns are displayed in the following sequence. When the ENTER key is pressed, the next pattern is displayed.

(i) The test pattern below is displayed.

DOT DISPLAY : 0 1 2 3 4 5 6 7 8 9 ; A a B b C

7SEG DISPLAY : 0. 1. 2. 3. 4. 5. 6. 7. 8. 9. -.

▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼ ▼

(ii) The screen displays a test pattern showing that all digits are lit.

② Display

```
Rear Display Check
```

③ Terminating procedure

Press the CANCEL key to turn off all the elements of the rear display.

3-8. SHARP Retail Network Diagnostics

The SRN test is performed.

To perform this test, the following composition is required.

- ER-A770
- Terminal resistor
- Branch (trunk) cable (only for data transfer test)

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the individual diagnostics program is completed, the display returns to this menu screen. When the CANCEL key is pressed, the display returns to the diagnostics menu.

```
SRN Diagnostics

  Self Check
  Flag Send Check
  Data Send Check
  Data Check (Satellite Machine)
  Data Check (Master Machine)
```

1) SRN Self Check

① Check content

The ROM and RAM for SRN are checked, and CTC interruption and carrier sense are checked. Also ADLC function and transmission/reception DMA check is made by using the self loop function of ADLC (MC6854). In addition, the other signals are checked. The check procedure is as follows:

- Execute diagnostics command 2. The number of resending is displayed.
- Execute diagnostics command 0. The error status is displayed. The error status is as shown in the table below. When an error occurs in this test, the following tests are not performed.

b7	An error occurs. (The error print is always 1.)
b6	An unexpected interruption is made.
b5	A collision is generated.
b4	An interruption of send complete cannot be made. (DMAC TC UP interruption)
b3	An interruption of carrier OFF cannot be made. The mirror image of carrier OFF shows carrier ON.
b2	An interruption of CTC CH2 or CH3 cannot be made. (Timer interruption)
b1	ROM sum check error
b0	RAM error

- Execute diagnostics command 1. The error status is displayed. The error status is as shown in the table below.

b7	An error is generated. (The error print is always 1.)
b6	An unexpected interruption is generated.
b5	DMA sent data and received data are different.
b4	The number of data received in DMA is abnormal.
b3	The number of data transmitted in DMA is abnormal.
b2	An overrun error is generated.
b1	An underrun error is generated.

b0	An interruption of send complete cannot be made. (DMAC TC UP interruption)

- Execute diagnostics command 5. The error status is displayed. The names and the directions of the signals which are subject to diagnostics 5 command are as shown in the table below.

Signal name	Direction
Power interruption notice	Host → Controller
Power interruption ON initialization	Host → Controller
Power interruption ON continuation	Host → Controller
Power interruption process complete	Host ← Controller
CH1 reception data present.	Host ← Controller
CH2 reception data present.	Host ← Controller

Check that the target bit of two statuses obtained by diagnostics 5 command is "0" for ST1 and "1" for ST2. (The other bits must be masked.) In the other cases, the error status is displayed with the error occurrence bit as "1." The normal bit shows "0."

The error status from the host to the controller is as shown in the table below.

b7	Not used. ("0" is always displayed.)
b6	Power interruption notice
b5	Not used. ("0" is always displayed.)
b4	Not used. ("0" is always displayed.)
b3	Not used. ("0" is always displayed.)
b2	Not used. ("0" is always displayed.)
b1	Power ON continuation
b0	Power ON initializing

The error status from the controller to the host is as shown in the table below.

b7	Not used. ("0" is always displayed.)
b6	Power interruption notice
b5	Not used. ("0" is always displayed.)
b4	CH2 reception data exits.
b3	CH1 reception data exits.
b2	Power interruption process complete
b1	Not used. ("0" is always displayed.)
b0	Not used. ("0" is always displayed.)

② Display

```
SRN Self Check
 DATA RETRY CNT.=xxx
 ACK  RETRY CNT.=xxx      The number of resending is displayed in xxx with a decimal number.
 DIAG 0      :xxxxxxxx    In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
 DIAG 1      :xxxxxxxx    In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
 DIAG 5 H→C  :xxxxxxxx    In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
 DIAG 5 H←C  :xxxxxxxx    In the sequence of b7, b6, ..., b0 from the left. "1" is displayed in case of an error, and "0" when normal.
```

③ Terminating procedure

Press the CANCEL key to terminate the check. After terminating, perform the service reset.

2) SRN Flag Send Check

① Check content

Execute diagnostics 3 command to send Flag (7EH) continuously.

② Display

```
SRN Flag Send Check
```

③ Terminating procedure

Perform the service reset.

3) SRN Data Send Check

① Check content

Execute diagnostics 4 command to send data of 00H ~ FFH (256Byte) as one packet at 12.8msec packet interval at 1Mbps continuously.

② Display

```
SRN Data Send Check
```

③ Terminating procedure

Perform the service reset.

4) Data Transmission Check

Data transmission is checked in an actually composed system. The system is composed of one master machine and max. 15 satellite machines.

Note for starting the check

- When checking the set in which the SRN setting has been made, cancel the SRN setting before starting this check.
- When checking the actually composed system, disconnect the SRM cables of the sets which are not checked, or cancel the SRN setting. If it is set to "SRN exits," data may be destroyed.
- The transmission check setting must be performed after canceling the SRN setting of all the sets in the system. First, set the satellite machines, then set the master machine.

① Setting procedure

- Satellite machine setting

In the menu screen, select "Data Transmission Check (Satellite)."

The display is as follows:

```
Data Transmission Check (Satellite)

   Input Terminal Number  :
```

Enter the terminal No. (000 ~ 254, 3 digits) of the machine to be checked and press the ENTER key. The display is as shown below.

```
Data Transmission Check (Satellite)

   Input Terminal Number : xxx   — The entered terminal No. is displayed.
   Data Sequence Number  : 0000
```

- Master machine setting

  In the menu screen, select "Data Transmission Check (Master)." The display is as shown below.

```
Data Transmission Check (Master)

   Input Master Terminal Number :
```

  Enter the terminal No. (000 ~ 254, 3 digits) of the machine to be checked and press the ENTER key. The display is as shown below.

```
Data Transmission Check (Master)

   Input Master Terminal Number    :xxx — The entered
   Input Satellite Terminal Number:       terminal No.
                                          is displayed.
```

  Enter the terminal No. (000 ~ 254, 3 digits) of the machine to be connected to the machine to be checked and press the ENTER key. The display is as shown below.

```
Data Transmission Check (Master)

   Input Master Terminal Number    :xxx
   Input Satellite Terminal Number:xxx — The entered
                                         terminal No.
                                         of satellite
                                         machine is
                                         displayed.
```

  When checking with two or more satellite machines connected, enter the terminal No. (000 ~ 254, 3 digits) and press the ENTER key similarly. To execute, press the ENTER key without entering the terminal No. The display is as shown below. Do not use the same terminal No. for different machines (master/satellite).

```
Data Transmission Check (Master)

   Input Master Terminal Number    : xxx
   Input Satellite Terminal Number : xxx
   xxx xxx xxx xxx xxx

   Data Sequence Number            : 0000
```

  With the above setting, data transmission between the master machine and the satellite machine is started.

② Check content

- Data in the following format composed of 2byte sequence No. and 254byte AAH data are transmitted from the master machine to the satellite machine. The master machine displays the sequence No.

1	2	3	4	5	•••	•••	•••	254	255	256	Byte
XX	XX	AA	AA	AA	•••	•••	•••	AA	AA	AA	

XXXX : Sequence No. (2byte: 4digits of binary decimal numbers)
AA : Transmission data (AAH) x 254 bytes

- The satellite machine sends back the received data to the master machine. The satellite machine displays the received sequence No.
- The master machine receives the data, and checks the sequence No. and 256byte AAH data. In case of an error, the master machine displays an error code and terminates the check. If two or more satellite machines are used, the above operation is repeated. If data transmission with all the satellite machines are normally completed, the master machine increments the sequence No.
  The above operation is repeated.

③ Error display

```
Data Transmission Check (Master)

   Input Master Terminal Number     : xxx
   Input Satellite Terminal Number  : xxx
   xxx xxx xxx xxx xxx

   Data Sequence Number             : xxxx
   IRC Error                        : xx —— The
                                           error
                                           code is
                                           displayed
```

The error codes are as shown below.

01	Command abnormality (except for during transmission)
02	No data received.
03	Received data present. Received data remained.
04	Remote station not ready (in sending) "NTDY" is sent back because the remote station is not ready for reception.
05	Reception buffer full (in sending) The controller reception buffer of the remote machine is full.
06	Resend error (in sending) Retry over (5 times) when no response
07	Collision error (in sending) When an collision occurred in data transmission
08	Line busy time out Transmission cannot be made by multi-station communication to cause time out in data send wait time.
09	Reception size over (in receiving) The reception buffer size is insufficient.
0A	Hardware error Interface abnormality (No SRN interface or abnormality in SRN controller)

④ Terminating procedure

Press the CANCEL key to terminate the check. After terminating, perform the service reset.

3-9. EFT Diagnostics

Perform EFT (ER-02EF) CHECK.

Select EFT Diag from the MENU and turn the Power OFF.

Press the CANCEL key to return to the Diag menu screen.

```
EFT Diagnostics
```

1) EFT Check

Set all DIPSW1 switches on the ER-02EF to OFF,turn the power of the system ON. EFT CHECK will be automatically performed.

① Details of the test

(1) For EFT CONNECTER,the LOOPBACK TEST is carried out on ER-DR,ER-CI,RS-CS.

(2) Check DIPSW1 by turning SWITCHES 1-8 ON one by one.

(3) When all switches are normal, SUM CHECK is carried out on EFT ROM,while WRITE/READ CHECK is carried out on RAM.

② Display (Normal end)

```
DIAGO(SELF TEST)      :OK
VHI27040R**1*         :OK
256K SRAM             :OK
```

③ Display (Error end)

```
In Loop Back Error
  ER-DR LOOP ERROR
  ER-CI LOOP ERROR
  RS-CS LOOP ERROR
In Self Test Error
  DIP SW ERROR
In Self Test Error
  VHI27040R**1*       :ERROR
  256K SRAM           :ERROR
```

④ Exit the Diag program.

Press the CANCEL key to exit the program.

3-10. Magnetic Card Reader Diagnostics

Read check of the optional UP-E12MR is performed.

The test program reads the magnetic card of ISO 7811/1-5 standard and displays the data. When the CANCEL key is pressed, the display returns to the diagnostics menu.

1) Magnetic Card Reader Check

① Check content

The test program reads tracks 1 and 2 of the magnetic card of ISO 7811/1-5, and displays the data in ASCII code.

② Display

```
   MCR (Magnetic Card Reader) Check
     TRACK1:
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
xxxxxxxxxx
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
     TRACK2:
xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

XXXXX shows the data read by the MCR. Incase of an error, the error code is displayed as shown below.

```
Magnetic Card Reader Check

   TRACK1:BUFFER EMPTY  ——— Displayed when TRACK1 empty
                            code is sent back.
   TRACK1:MCR ERROR     ——— Displayed when TRACK1 empty
                            code is sent back.
   TRACK2:BUFFER EMPTY  ——— Displayed when TRACK2 empty
                            code is sent back.
   TRACK2:MCR ERROR     ——— Displayed when TRACK2 empty
                            code is sent back.
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

3-11. Drawer Diagnostics

This diagnostics is used to check the drawer open and sensors.

The following menu is displayed. The cursor position is highlighted. Use ↑ key and ↓ key to move the cursor. Move the cursor to the process you desire and press the enter key. The selected individual diagnostics program is executed. When the CANCEL key is pressed, the display returns to the diagnostics menu.

```
Drawer Diagnostics
   Drawer 1 Check
   Drawer 2 Check
```

1) Drawer 1 Check

① Check content

The solenoid of drawer 1 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

② Display

```
Drawer 1 Check
   Drawer Open Sensor  :  OPEN (or CLOSE)
```

③ Terminating procedure

Press the CANCEL key to terminate the check.

2) Drawer 2 Check

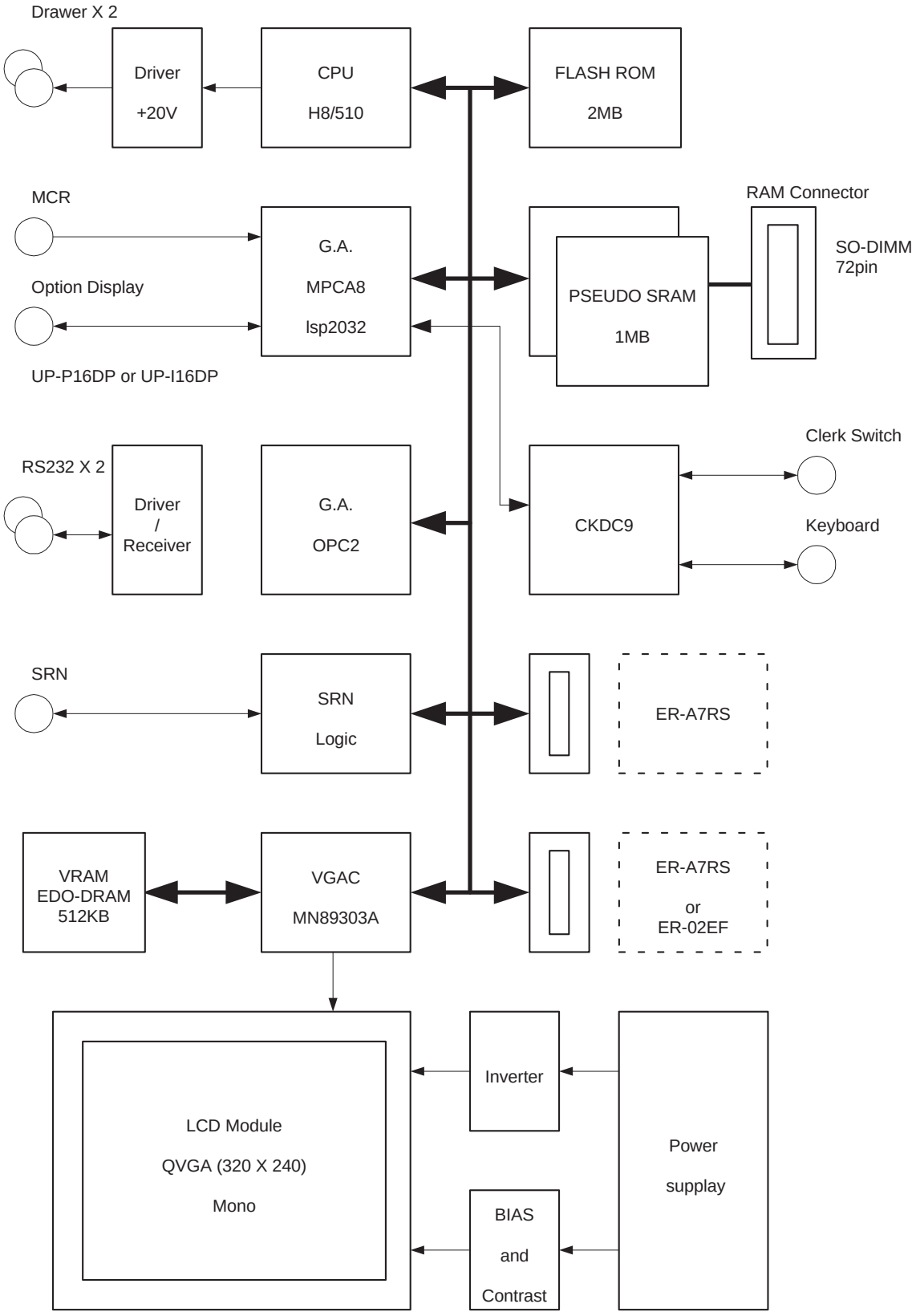
① Check content

The solenoid of drawer 2 is turned on, and the drawer open sensor value is sensed at every 100ms, and the state is displayed.

The display and the terminating procedure are the same as Drawer 1 Check.

CHAPTER 7. CIRCUIT DESCRIPTION

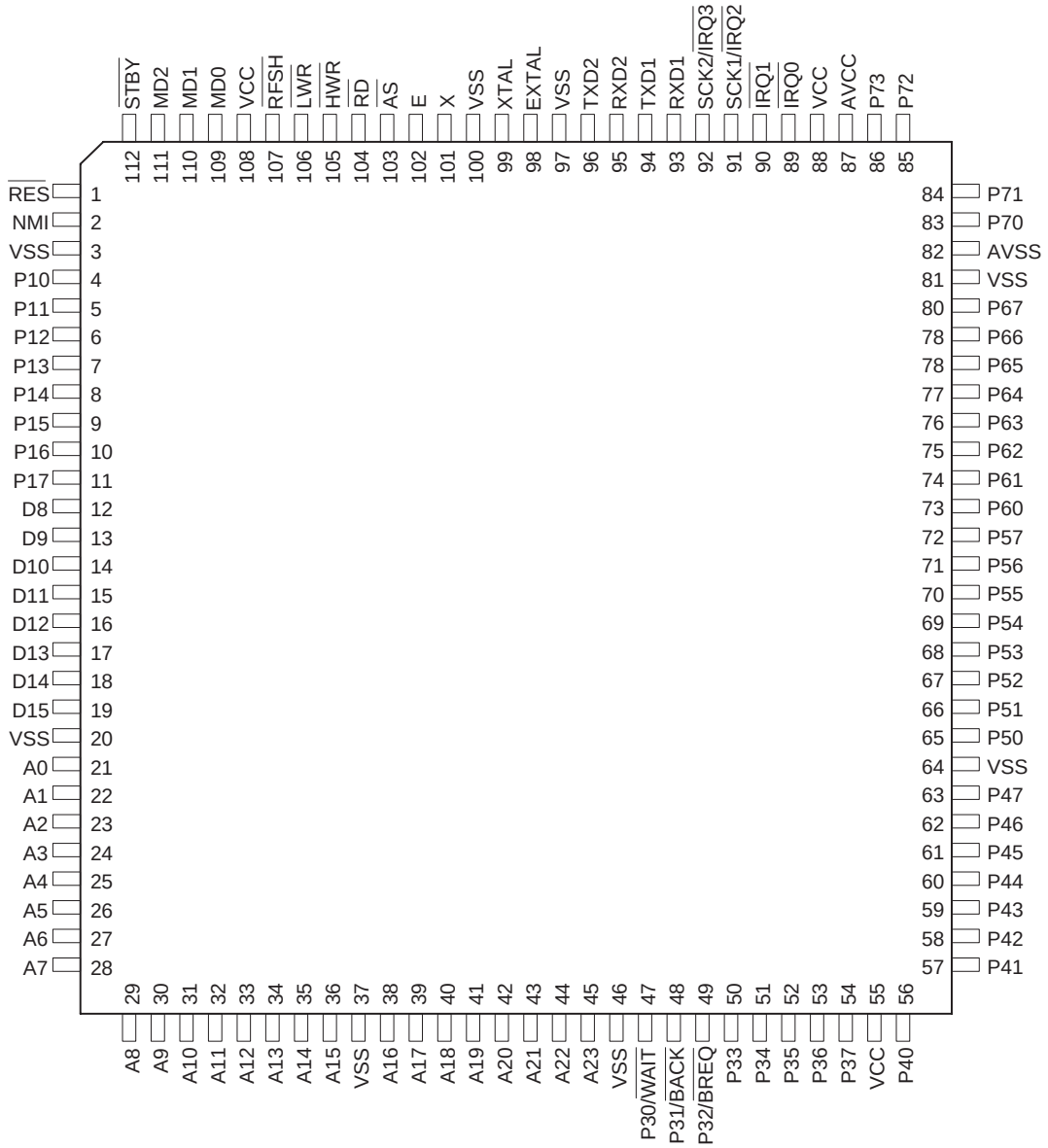
1. Hardware block diagram



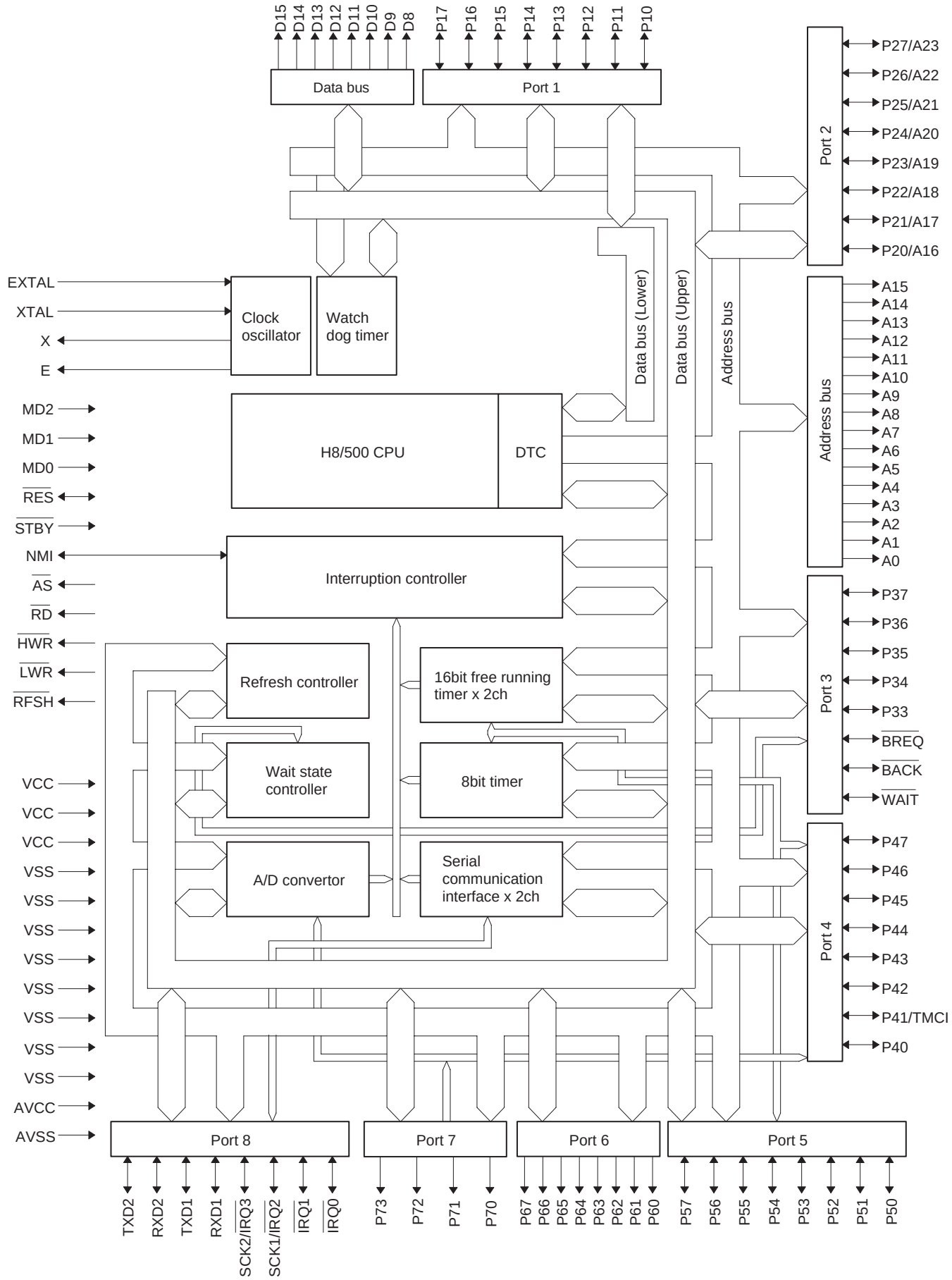
2. Description of main LSI's

2-1. CPU (HD6415108FX)

1) Pin description



2) Block diagram



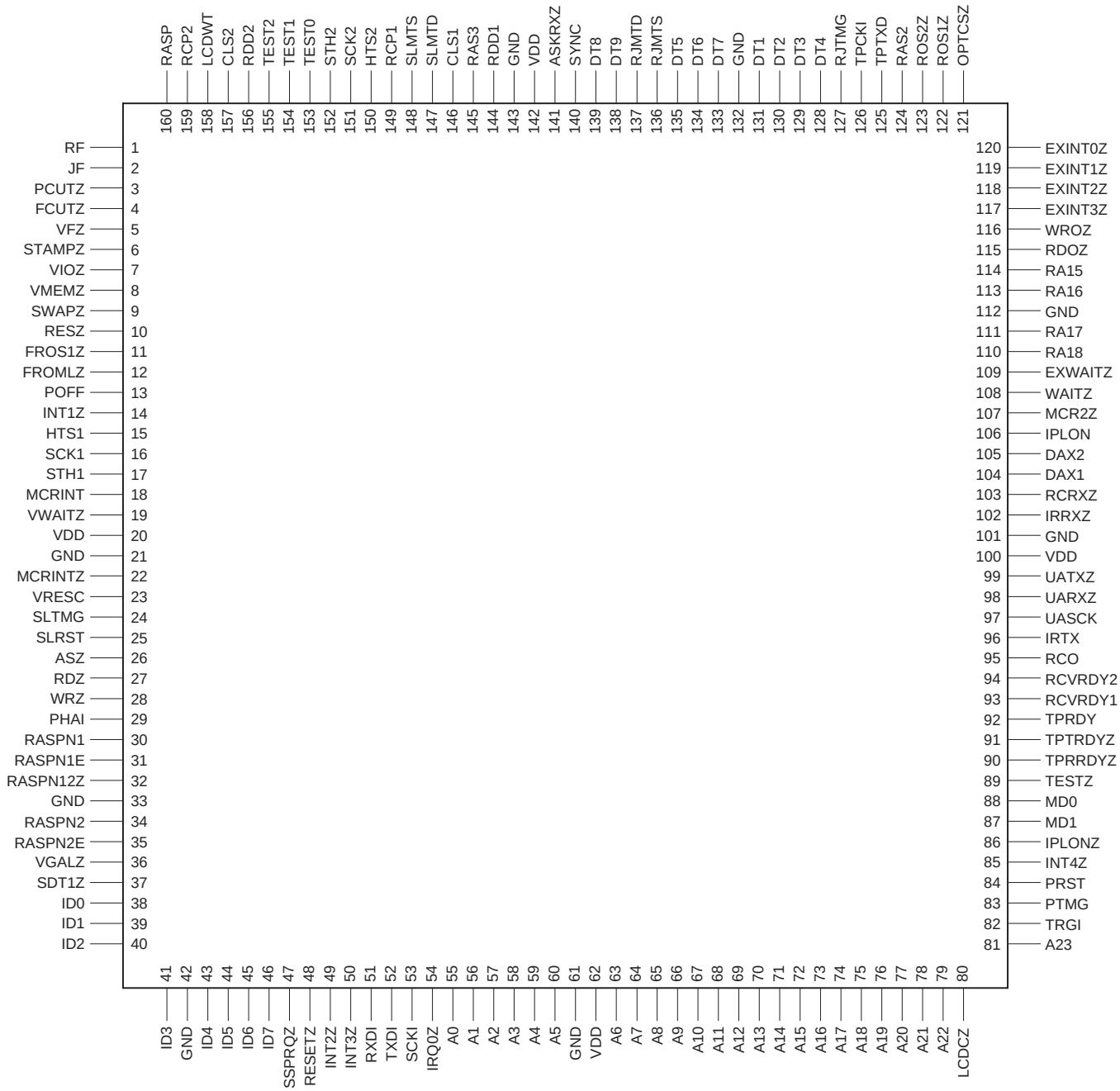
3) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	/RES	/RESET	In	Reset signal
2	NMI	NMI	In	Non-maskable interrupt input for SSP interrupt input.
3	VSS	GND	In	GND
4	D0	D0	I/O	Data bus
5	D1	D1	I/O	Data bus
6	D2	D2	I/O	Data bus
7	D3	D3	I/O	Data bus
8	D4	D4	I/O	Data bus
9	D5	D5	I/O	Data bus
10	D6	D6	I/O	Data bus
11	D7	D7	I/O	Data bus
12	D8	D8	I/O	Data bus
13	D9	D9	I/O	Data bus
14	D10	D10	I/O	Data bus
15	D11	D11	I/O	Data bus
16	D12	D12	I/O	Data bus
17	D13	D13	I/O	Data bus
18	D14	D14	I/O	Data bus
19	D15	D15	I/O	Data bus
20	VSS	GND	In	GND
21	A0	A0	Out	Address bus
22	A1	A1	Out	Address bus
23	A2	A2	Out	Address bus
24	A3	A3	Out	Address bus
25	A4	A4	Out	Address bus
26	A5	A5	Out	Address bus
27	A6	A6	Out	Address bus
28	A7	A7	Out	Address bus
29	A8	A8	Out	Address bus
30	A9	A9	Out	Address bus
31	A10	A10	Out	Address bus
32	A11	A11	Out	Address bus
33	A12	A12	Out	Address bus
34	A13	A13	Out	Address bus
35	A14	A14	Out	Address bus
36	A15	A15	Out	Address bus
37	VSS	GND	In	GND
38	A16	A16	Out	Address bus
39	A17	A17	Out	Address bus
40	A18	A18	Out	Address bus
41	A19	A19	Out	Address bus
42	A20	A20	Out	Address bus
43	A21	A21	Out	Address bus
44	A22	A22	Out	Address bus
45	A23	A23	Out	Address bus
46	VSS	GND	In	GND
47	P30	/WAIT	In	Wait signal
48	P31	/BACK	Out	Bus control request acknowledge signal
49	P32	/BREQ	In	Bus control request signal
50	P33	DOPS	In	Drawer open signal
51	P34	/DR0	Out	Option drawer open signal
52	P35	/DR1	Out	Option drawer open signal
53	P36	NC	NC	NC
54	P37	NC	NC	NC
55	VCC	VCC	In	+5V
56	P40	VCC	In	+5V
57	P41	GND	In	GND
58	P42	GND	In	GND

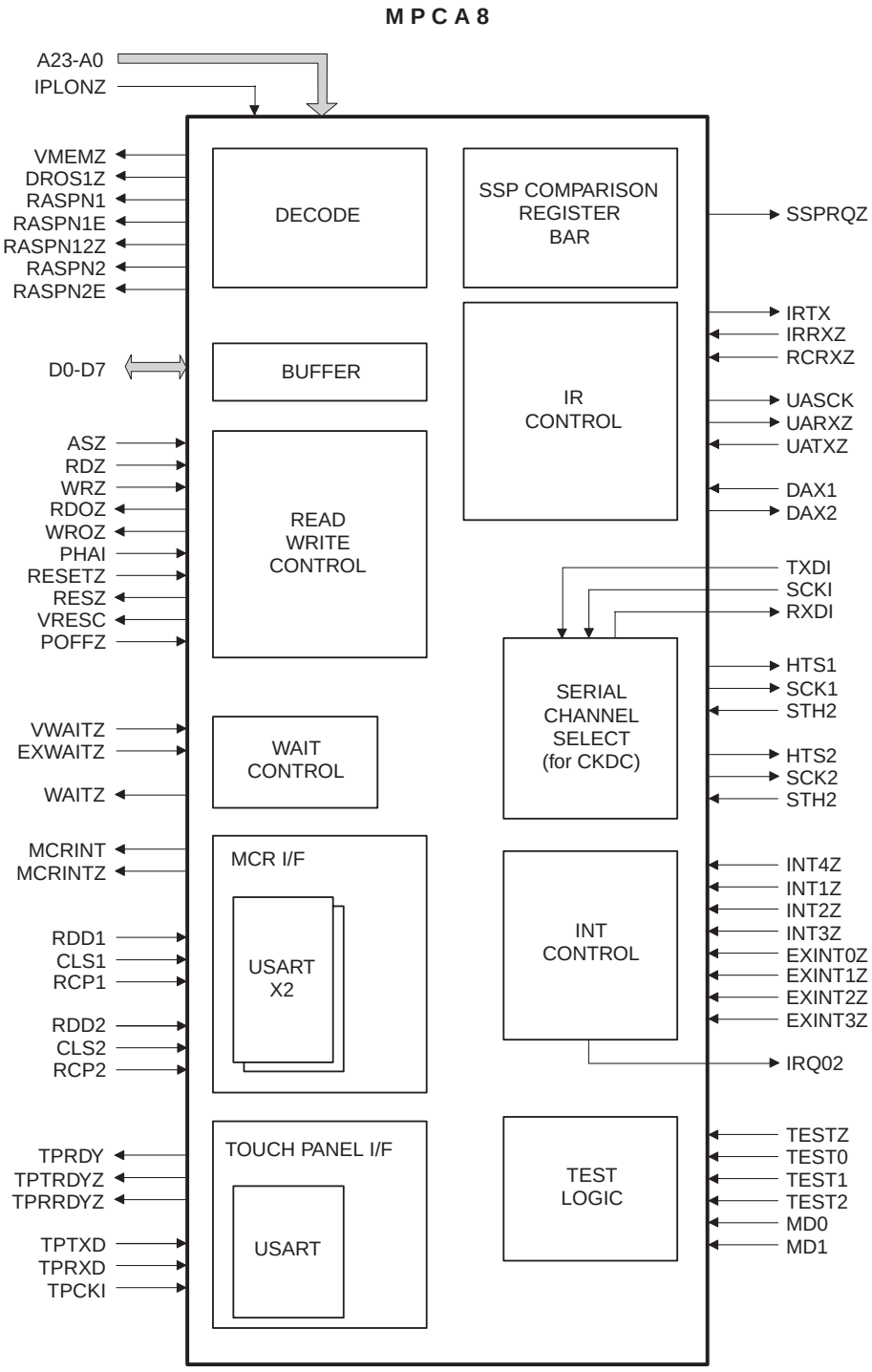
Pin No.	Symbol	Signal name	In/ Out	Function
59	P43	GND	In	GND
60	P44	MCRINT	In	MCR interrupt signal
61	P45	GND	In	GND
62	P46	/SHEN	In	CKDC interface shift enable signal
63	P47	GND	In	GND
64	VSS	GND	In	GND
65	P50	–	Out	/DTR2 : Data Terminal Ready2
66	P51	–	In	/DSR2 : Data Set Ready2
67	P52	–	In	/CTS2 : Clear To Send2
68	P53	–	In	/DCD2 : Carriar Detect2
69	P54	–	In	NC
70	P55	NC	Out	/RTS2:Request To Send2
71	P56	–	In	/CI2:Calling Indicator2
72	P57	/STOP	Out	System reset output signal
73	P60	/IPLON0	In	From IPL SW of ER-A7RS
74	P61	/IPLON1	In	From IPL SW of ER-A770
75	P62	GND	In	GND
76	P63	NORDY	In	Flash Memory ready ("H" active)
77	P64	FVPON	Out	Flash Memory write protect ("L" active)
78	P65	BANK	Out	For IPL ROM
79	P66	GND	In	GND
80	P67	GND	In	GND
81	VSS	GND	In	GND
82	AVSS	GND	In	GND
83	P70	GND	In	GND
84	P71	GND	In	GND
85	P72	GND	In	GND
86	P73	GND	In	GND
87	AVCC	VCC	In	+5V
88	VCC	VCC	In	+5V
89	/IRQ0	/IRQ0	In	Interrupt signal 0
90	/IRQ1	/IRQ1	In	Interrupt signal 1
91	/IRQ2	UASCK	In	Synchronizing shift clock signal for USART
92	/IRQ3	SCKI	Out	CKDC interface synchronizing shift clock
93	RXD1	/RCVDT2	In	RXD signal for RS232
94	TXD1	TXD2	Out	TXD signal for RS232
95	RXD2	RXDI	In	CKDC interface shift input data
96	TXD2	TXDI	Out	CKDC interface shift output data
97	VSS	GND	In	GND
98	EXTAL	EXTAL	In	Crystal oscillator connection 19.6MHz
99	XTAL	XTAL	In	Crystal oscillator connection 19.6MHz
100	VSS	GND	In	GND
101	X	#	Out	System clock
102	E	NC	NC	NC
103	/AS	/AS	Out	Address strobe
104	RD	/RD	Out	Read signal
105	/HWR	/HWR	Out	Write signal (HIGH)
106	/LWR	/LWR	Out	Write signal (LOW)
107	/RFSH	/RFSH	Out	Refresh cycle signal
108	VCC	VCC	In	+5V
109	MD0	IPLON0	In	From IPL SW of ER-A7RS
110	MD1	IPLON0	In	From IPL SW of ER-A7RS
111	MD2	/IPLON0	In	From IPL SW of ER-A7RS
112	/STBY	VCC	In	+5V

2-2. G.A.(MPCA8)

1) Pin configuration



2) Block diagram



3) Pin description

Pin No.	Name	I/O	Description
1	RF	ON	NU
2	JF	ON	NU
3	PCUTZ	ON	NU
4	FCUTZ	ON	NU
5	VFZ	ON	NU
6	STAMPZ	ON	NU
7	VIOZ	O	NU
8	VMEMZ	O	VRAM DEOCDE
9	SWAPZ	O	NU
10	RESZ	O6M	RESET
11	FROS1Z	O	FLASH ROM DECODE
12	FROMLZ	O	NU
13	POFF	IC	POWER OFF SIGNAL INPUT
14	INT1Z	ICU	INTERRUPT SIGNAL INPUT
15	HTS1	O	SERIAL OUT (CKDC INTERFACE)
16	SCK1	O	SERIAL CLOCK (CKDC INTERFACE)
17	STH1	IS	SERIAL IN (CKDC INTERFACE)
18	MCRINT	O	MCR INTRRUPT OUT
19	VWAITZ	IU	VGA WAIT INPUT
20	VDD	–	
21	GND	–	
22	MCRINTZ	O	MCR INTRRUPT OUT
23	VRESC	ON	TURNS ACTIVE WHEN RESET&POWER DOWN IS MET
24	SLTMG	ICS	GND
25	SLRST	ICS	GND
26	ASZ	I	ADDRESS STROBE
27	RDZ	I	READ STROBE
28	WRZ	I	WRITE STROBE
29	PHAI	IS	SYSTEM CLOCK (9.83MHz)
30	RASPN1	O	PSRAM DECODE1
31	RASPN1E	O	PSRAM DECODE1 (EVEN)
32	RASPN12Z	O	PSRAM DECODE1 OR 2
33	GND	–	
34	RASPAN2	O	PSRAM DECODE2
35	RASPN2E	O	PSRAM DECODE2(EVEN)
36	VGALZ	O	NU
37	SDT1Z	O	NU
38	ID0	IO	DATA BUS
39	ID1	IO	DATA BUS
40	ID2	IO	DATA BUS
41	ID3	IO	DATA BUS
42	GND	–	
43	ID4	IO	DATA BUS
44	ID5	IO	DATA BUS
45	ID6	IO	DATA BUS
46	ID7	IO	DATA BUS
47	SSPRQZ	O	SSP REQUEST FOR CPU
48	RESETZ	ICS	MPCA RESET
49	INT2Z	ICU	INTERRUPT INPUT (NU)
50	INT3Z	ICU	INTERRUPT INPUT (NU)
51	RXDI	O	SERIAL OUT FOR CPU
52	TXDI	IS	SERIAL IN FROM CPU
53	SCKI	IU	SERIAL CLOCK FROM CPU

Pin No.	Name	I/O	Description
54	IRQ0Z	O	INTERRUPT SIGNAL FOR CPU
55	A0	I	ADDRESS BUS
56	A1	I	ADDRESS BUS
57	A2	I	ADDRESS BUS
58	A3	I	ADDRESS BUS
59	A4	I	ADDRESS BUS
60	A5	I	ADDRESS BUS
61	GND	–	
62	VDD	–	
63	A6	I	ADDRESS BUS
64	A7	I	ADDRESS BUS
65	A8	I	ADDRESS BUS
66	A9	I	ADDRESS BUS
67	A10	I	ADDRESS BUS
68	A11	I	ADDRESS BUS
69	A12	I	ADDRESS BUS
70	A13	I	ADDRESS BUS
71	A14	I	ADDRESS BUS
72	A15	I	ADDRESS BUS
73	A16	I	ADDRESS BUS
74	A17	I	ADDRESS BUS
75	A18	I	ADDRESS BUS
76	A19	I	ADDRESS BUS
77	A20	I	ADDRESS BUS
78	A21	I	ADDRESS BUS
79	A22	I	ADDRESS BUS
80	LCDCZ	O	NU
81	A23	I	ADDRESS BUS
82	TRGI	IS	NU
83	PTMG	O	NU
84	PRST	O	NU
85	INT4Z	ICU	INTERRUPT INPUT (SHEN2 FOR OPTION CKDC)
86	IPLONZ	IU	IPL SIGNAL FROM OPTION CONNECTER
87	MD1	ICU	TEST PIN
88	MD0	ICU	TEST PIN
89	TESTZ	ICU	TEST PIN
90	TPRRDYZ	O	NU
91	TPTRDYZ	O	NU
92	TPRDY	O	NU
93	RCVRDY1	IU	NU
94	RCVRDY2	IU	NU
95	RCO	O	NU
96	IRTX	O	NU
97	UASCK	O	USART CLOCK
98	UARXZ	O	NU
99	UATXZ	IU	NU
100	VDD	–	
101	GND	–	
102	IRRXZ	ICS	NU
103	RCRXZ	ICS	NU
104	DAX1	OSCI	IR CLOCK (7.37MHz)

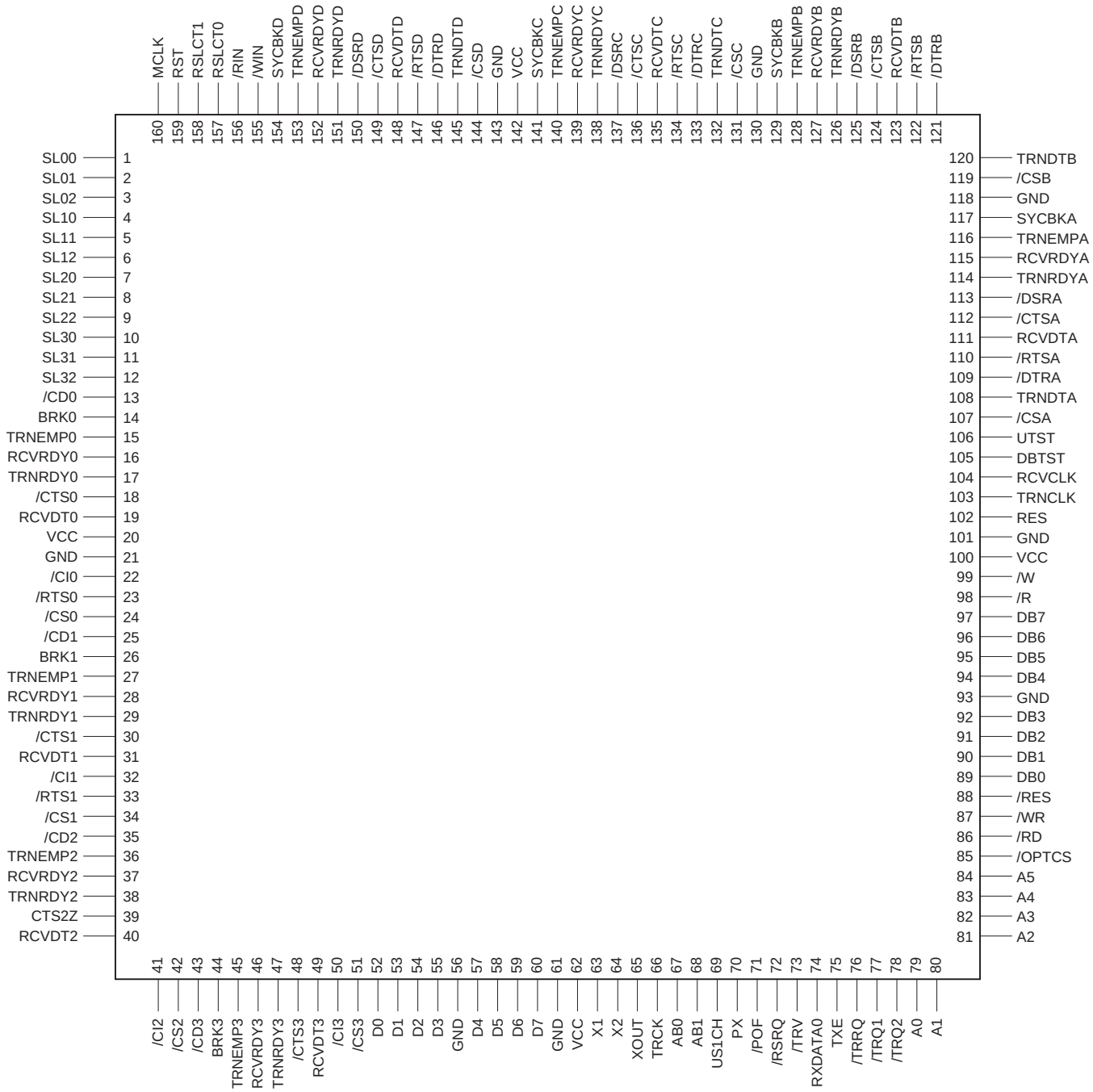
Pin No.	Name	I/O	Description
105	DAX2	OSCO	IR CLOCK (7.37MHz)
106	IPLON	O	IPLON SIGNAL
107	MCR2Z	O	NU
108	WAITZ	O	WAIT FOR CPU
109	EXWAITZ	IU	EXTERNAL WAIT INPUT SIGNAL
110	RA18	O	NU
111	RA17	O	NU
112	GND	–	
113	RA16	O	NU
114	RA15	O	NU
115	RDOZ	O8M	EXPANSION RD
116	WROZ	O8M	EXPANSION WR
117	EXINT3Z	ICS	EXPANSION INTERRUPT SIGNAL
118	EXINT2Z	ICS	EXPANSION INTERRUPT SIGNAL
119	EXINT1Z	ICS	EXPANSION INTERRUPT SIGNAL
120	EXINT0Z	ICS	EXPANSION INTERRUPT SIGNAL
121	OPTCSZ	O	BASE DECODE SIGNAL FOR EXPANSION SLOT
122	ROS1Z	O	NU
123	ROS2Z	O	N U
124	RAS2	O	NU
125	TPTXD	O	NU
126	TPRXD	ICS	NU
127	TPCKI	ICS	NU
128	DT4	ON	NU
129	DT3	ON	NU
130	DT2	ON	NU
131	DT1	ON	NU
132	GND	–	
133	DT7	ON	NU
134	DT6	ON	NU
135	DT5	ON	NU
136	RJMTS	ON	NU
137	RJMTD	ON	NU
138	DT9	ON	NU
139	DT8	ON	NU
140	SYNC	IU	NU
141	ASKRXZ	ICS	NU
142	VDD	–	
143	GND	–	
144	RDD1	ICS	SERIAL IN FROM MCR TRACK1
145	RAS3	O	NU
146	CLS1	ICS	CARD SENSE ON MCR TRACK1
147	SLMTD	ON	NU
148	SLMTS	ON	NU
149	RCP1	ICS	CLOCK PULSE FROM MCR TRACK1
150	HTS2	O	SERIAL OUT (OPTION CKDC INTERFACE)
151	SCK2	O	SERIAL CLOCK (OPTION CKDC INTERFACE)
152	STH2	IS	SERIAL IN (OPTION CKDC INTERFACE)
153	TEST0	I	TEST PIN
154	TEST1	I	TEST PIN
155	TEST2	I	TEST PIN

Pin No.	Name	I/O	Description
156	RDD2	ICS	SERIAL IN FROM MCR TRACK1
157	CLS2	ICS	CARD SENSE ON MCR TRACK1
158	LCDWT	IU	NU
159	RCP2	ICS	CLOCK PULSE FROM MCR TRACK1
160	RASP	O	NU

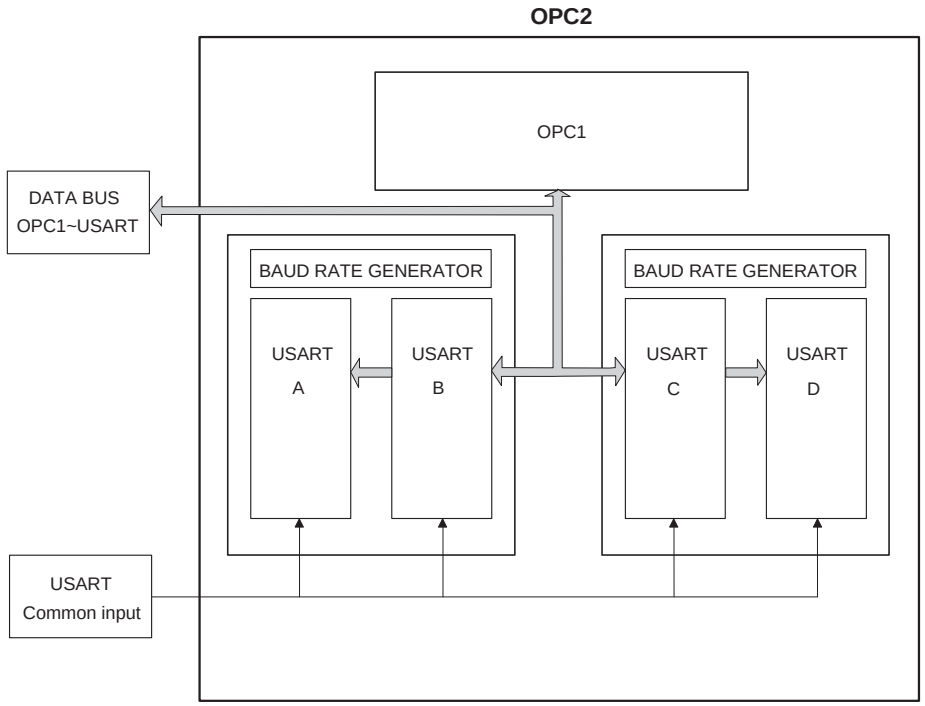
I	TTL input
IS	TTL Schmidt input
IU	TTL pull up input
IC	CMOS input
ICS	CMOS Schmidt input
ICU	CMOS pull up input
IO	TTL I/O
O	Output 4mA
O8M	Output 8mA
ON	Nch open drain output
OSIC	Oscillation circuit input
OSCI	Oscillation circuit output

2-3. OPC2

1) Pin configuration



2) Block diagram



3) Pin description

Pin NO.	Name	ER-A770	I/O	Description
1	SL00	VCC	ISU	RS-232/UNIT0 channel select
2	SL01	GND	ISU	
3	SL02	GND	ISU	
4	SL10	GND	ISU	RS-232/UNIT1 channel select
5	SL11	GND	ISU	
6	SL12	GND	ISU	
7	SL20	GND	ISU	RS-232/UNIT2 channel select
8	SL21	GND	ISU	
9	SL22	GND	ISU	
10	SL30	GND	ISU	RS-232/UNIT3 channel select
11	SL31	GND	ISU	
12	SL32	GND	ISU	
13	/CD0	/DCD1	IS	RS-232 control signal /CD input
14	BRK0	BRK1	IS	RS-232 break signal
15	TRNEMP0	TRENMP1	IS	RS-232 transmission buffer empty signal
16	RCVRDY0	RCVRDY1	IS	RS-232 data reception enable signal
17	TRNRDY0	TRNRDY1	IS	RS-232 transmission enable signal
18	/CTS0	/CTS1	IS	RS-232 clear to send signal
19	RCVDT0	RCVDT1	IS	RS-232 reception data signal
20	VCC	VCC		+5V
21	GND	GND		GND
22	/CI0	/CI1	IS	RS-232 control signal /CI input
23	/RTS0	/RTS1	O	RS-232 request to send signal

Pin NO.	Name	ER-A770	I/O	Description
24	/CS0	/CS1	O	RS-232 chip select signal
25	/CD1	/DCD2	IS	RS-232 control signal /CD input
26	BRK1	BRK2	IS	GND
27	TRNEMP1	TRENMP2	IS	GND
28	RCVRDY1	RCVRDY2	IS	GND
29	TRNRDY1	TRNRDY2	IS	GND
30	/CTS1	/CTS2	IS	+5V
31	RCVDT1	RCVDT2	IS	RS-232 reception data signal
32	/CI1	/CI2	IS	RS-232 control signal /CI input
33	/RTS1	/RTS2	O	RS-232 request to send signal
34	/CS1	/CS2	O	RS-232 chip select signal
35	/CD2	VCC	IS	+5V
36	TRNEMP2	TRENMP3	IS	GND
37	RCVRDY2	RCVRDY3	IS	GND
38	TRNRDY2	TRNRDY3	IS	GND
39	CTS2Z	/CTS3	IS	+5V
40	RCVDT2	RCVDT3	IS	GND
41	/CI2	VCC	IS	+5V
42	/CS2	/CS3	O	NU
43	/CD3	/SINT	IS	RS-232: /CD, IN-LINE : /P1
44	BRK3	GND	IS	GND
45	TRNEMP3	GND	IS	GND
46	RCVRDY3	GND	IS	GND
47	TRNRDY3	GND	IS	GND

Pin NO.	Name	ER-A770	I/O	Description
48	/CTS3	GND	IS	GND
49	RCVDT3	GND	IS	GND
50	/CI3	GND	IS	GND
51	/CS3	/SRCS	O	RS-232/INLINE chip select signal
52	D0	D0	IO	Data bus (CPU)
53	D1	D1	IO	Data bus (CPU)
54	D2	D2	IO	Data bus (CPU)
55	D3	D3	IO	Data bus (CPU)
56	GND	GND		GND
57	D4	D4	IO	Data bus (CPU)
58	D5	D5	IO	Data bus (CPU)
59	D6	D6	IO	Data bus (CPU)
60	D7	D7	IO	Data bus (CPU)
61	GND	GND		GND
62	VCC	VCC		+5V
63	X1	NC	O OSI14	NC
64	X2	#	I OSI14	System clock
65	XOUT	CLK_USART	O	Clock (USART)
66	TRCK	NC	O	NC
67	AB0	AH0	O	Address bus for USART
68	AB1	AH1	O	Address bus for USART
69	US1CH	GND	IS	GND
70	PX	NC	O	NC
71	/POF	/POFF	IS	POFF signal
72	/RSRQ	/IRQ1	3S	RS232 INTRRUPT
73	/TRV	GND	IS	GND
74	RXDATA0	NC	O	NC
75	TXE	/SRESET	O	INLINE SOFT RESET
76	/TRRQ	/TRQ2	3S	INLINE INTRRUPT
77	/TRQ1	/TRQ1	ON6	TIMER INTRRUPT (RS232)
78	/TRQ2	NC	ON6	TIMER INTRRUPT (INLINE)
79	A0	A0	I	Address bus for CPU
80	A1	A1	I	Address bus for CPU
81	A2	A2	I	Address bus for CPU
82	A3	A3	I	Address bus for CPU
83	A4	A4	I	Address bus for CPU
84	A5	A5	I	Address bus for CPU
85	/OPTCS	/OPTCS	I	Option chip select (from MPCA)
86	/RD	/RDO	I	Read signal (from CPU)
87	/WR	/WRO	I	Write signal (from CPU)
88	/RES	/RES	IS	Reset signal (from CPU)
89	DB0	DB0	IO	DATA BUS (USART)
90	DB1	DB1	IO	DATA BUS (USART)
91	DB2	DB2	IO	DATA BUS (USART)
92	DB3	DB3	IO	DATA BUS (USART)
93	GND	GND		GND
94	DB4	DB4	IO	DATA BUS (USART)
95	DB5	DB5	IO	DATA BUS (USART)
96	DB6	DB6	IO	DATA BUS (USART)

Pin NO.	Name	ER-A770	I/O	Description
97	DB7	DB7	IO	DATA BUS (USART)
98	/R	/RDH	O	Read signal (to USART)
99	/W	/WRH	O	Write signal (to USART)
100	VCC	VCC		+5V
101	GND	GND		GND
102	RES	RES USART	O	Reset signal (to USART)
103	TRNCLK	GND	I	GND
104	RCVCLK	GND	I	GND
105	DBTST	/SRCS	ID	RS-232/INLINE USART chip select
106	UTST	VCC	ID	+5V
107	/CSA	/CS1	IS	USART_A chip select
108	TRNDTA	TXD1	O	RS-232 transmission data signal
109	/DTRA	/DTR1	O	RS-232 data terminal ready signal
110	/RTSA	NC	O	NC
111	RCVDTA	RCVDT1	IS	RS-232 reception data signal
112	/CTSA	GND	IS	GND
113	/DSRA	/DSR1	IS	RS-232 data set ready signal
114	TRNRDYA	TRNRDY1	O	RS-232 data transmission enable signal
115	RCVRDYA	RCVRDY1	O	RS-232 data reception enable signal
116	TRNEMPA	TRNEMP1	O	RS-232 transmission buffer empty signal
117	SYCBKA	BRK1	IO	Break code detection signal
118	GND	GND		GND
119	/CSB	/CS2	IS	USART_B chip select
120	TRNDTB	TXD2	O	NC
121	/DTRB	/DTR2	O	NC
122	/RTSB	NC	O	NC
123	RCVDTB	RCVDT2	IS	GND
124	/CTSB	GND	IS	GND
125	/DSRB	/DSR2	IS	GND
126	TRNRDYB	TRNRDY2	O	NC
127	RCVRDYB	RCVRDY2	O	NC
128	TRNEMPB	TRNEMP2	O	NC
129	SYCBKB	BRK2	IO	NC
130	GND	GND		GND
131	/CSC	/CS3	IS	USART_C chip select
132	TRNDTC	TXD3	O	NC
133	/DTRC	/DTR3	O	NC
134	/RTSC	/RTS3	O	NC
135	RCVDTC	RCVDT3	IS	GND
136	/CTSC	GND	IS	GND
137	/DSRC	/DSR3	IS	GND
138	TRNRDYC	TRNRDY3	O	NC
139	RCVRDYC	RCVRDY3	O	NC
140	TRNEMPC	TRNEMP3	O	NC
141	SYCBKC	NC	IO	NC

Pin NO.	Name	ER-A770	I/O	Description
142	VCC	VCC		+5V
143	GND	GND		GND
144	/CSD	VCC	IS	+5V
145	TRNDTD	NC	O	NC
146	/DTRD	NC	O	NC
147	/RTSD	NC	O	NC
148	RCVDTD	GND	IS	GND
149	/CTSD	GND	IS	GND
150	/DSRD	GND	IS	GND
151	TRNRDYD	NC	O	NC
152	RCVRDYD	NC	O	NC
153	TRNEMPD	NC	O	NC
154	SYCBKD	NC	IO	NC
155	/WIN	/WRH	I	Write signal
156	/RIN	/RDH	I	Read signal
157	RSLCT0	AH0	I	Address bus
158	RSLCT1	AH1	I	Address bus
159	RST	RES USART	IS	Reset signal
160	MCLK	CLK USART	I	Clock (4.91MHz)

I TTL input

ID TTL input with pull down

IS TTL Schmidt input

ISU TTL Schmidt input with pull up

IO TTL I/O

3S 3-state Buffer (6mA)

ON6 Open drain (6mA)

2-4. Z80 CPU

1) Features

The extensive instruction set contains 158 instructions, including the 8080A instruction set as a subset.

- NMOS version for low cost high performance solutions, CMOS version for high performance low power designs.
- Z0840006 - 6.17 MHz
- CMOS Z84C0006 - DC to 6.17 MHz, Z84C008 - DC to 8 MHz, Z84C0010 - DC to 10 MHz, Z84C0020 - DC - 20 MHz
- 6 MHz version can be operated at 6.144 MHz clock.
- The Z80 microprocessors and associated family of peripherals can be linked by a vectored interrupt system. This system can be daisy-chained to allow implementation of a priority interrupt scheme.
- Duplicate set of both general-purpose and flag registers.
- Two sixteen-bit index registers.
- Three modes of maskable interrupts:

  Mode 0 — 8080A similar;

  Mode 1 — Non-Z80 environment, location 38H;

  Mode 2 — Z80 family peripherals, vectored interrupts.
- On-chip dynamic memory refresh counter.

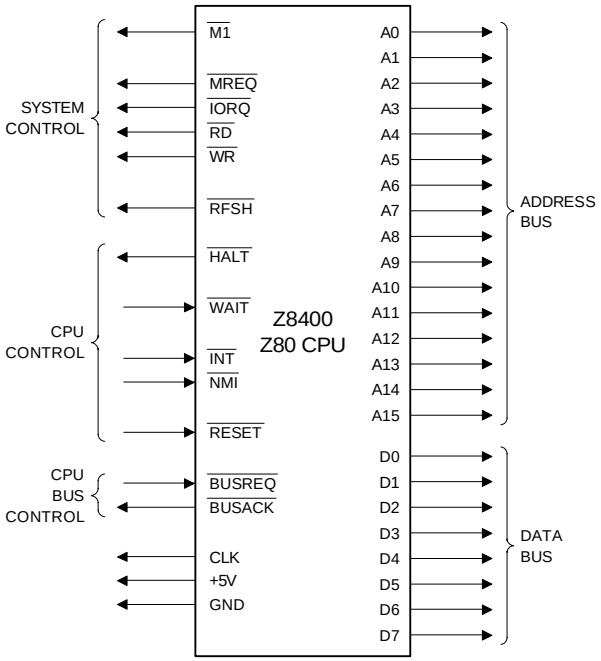
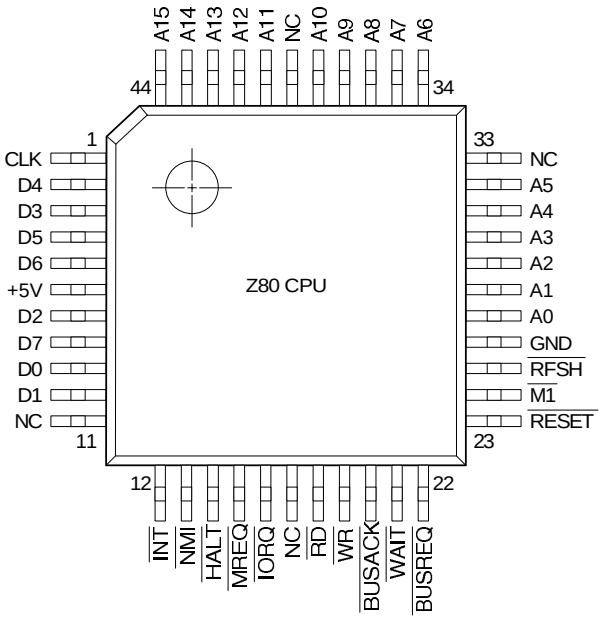


Figure 1. Pin functions

2) Pin configuration



44Pin Quad Flat Pack (QFP), Pin Assignments
(Only available for 84C00)

3) General description

The CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. Theinternal registers contain 208 bits of read/write memory that are accessible to the programmer.

These registers include two sets of six general-purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation inforeground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

The internal block diagram (Figure 3) shows the primary functions of the processors. Subsequent text provides more detail on the I/O controller family, registers, instruction set, interrupts and daisy chaining, and CPU timing.

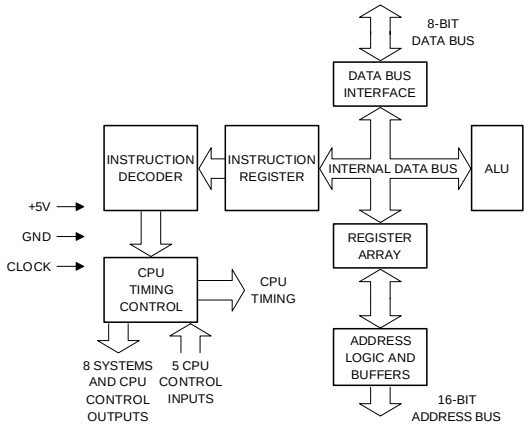


Figure 3. Z80C CPU Block Diagram

4) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	CLK	CLK	In	Clock
2	D4	S D4	In/Out	Data bus
3	D3	S D3	In/Out	Data bus
4	D5	S D5	In/Out	Data bus
5	D6	S D6	In/Out	Data bus
6	+5V	VCC	—	+5V
7	D2	S D2	In/Out	Data bus
8	D7	S D7	In/Out	Data bus
9	D0	S D0	In/Out	Data bus
10	D1	S D1	In/Out	Data bus
11	NC	NC	—	NC
12	$\overline{INT}$	S INT	In	Interrupt request signal
13	$\overline{NMI}$	VCC	—	Non-maskable interrupt signal
14	$\overline{HALT}$	VCC	—	+5V
15	$\overline{MREQ}$	S $\overline{MRQ}$	Out	Memory request signal
16	$\overline{IORQ}$	S $\overline{IORQ}$	Out	Input / Output request signal
17	NC	NC	—	NC
18	$\overline{RD}$	S $\overline{RDS}$	Out	Rread signal
19	$\overline{WR}$	S $\overline{WRS}$	Out	Write signal
20	$\overline{BUSAK}$	$\overline{BUSAK}$	Out	Bus acknowledge signal
21	$\overline{WAIT}$	S $\overline{WAIT}$	In	Wait signal
22	$\overline{BUSRQ}$	$\overline{BUSRQ}$	In	Bus request signal
23	$\overline{RESET}$	S $\overline{RES}$	In	Reset signal
24	$\overline{M1}$	S M1	Out	Machine cycle one signal
25	$\overline{RFSH}$	NC	—	NC
26	GND	GND	—	GND
27	A0	S A0	Out	Address bus
28	A1	S A1	Out	Address bus
29	A2	S A2	Out	Address bus
30	A3	S A3	Out	Address bus
31	A4	S A4	Out	Address bus
32	A5	S A5	Out	Address bus
33	NC	NC	—	NC
34	A6	S A6	Out	Address bus
35	A7	S A7	Out	Address bus
36	A8	S A8	Out	Address bus
37	A9	S A9	Out	Address bus
38	A10	S A10	Out	Address bus
39	NC	NC	—	NC
40	A11	S A11	Out	Address bus
42	A13	S A13	Out	Address bus
43	A14	S A14	Out	Address bus
44	A15	S A15	Out	Address bus

2-5. Z80 CTC

1) Features

- Four independently programmable counter/timer channels, each with a readable downcounter and a selectable 16 or 256 prescaler. Downcounters are reloaded automatically at zero count.
- Selectable positive or negative trigger initiates timer operation.
- Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors. (1.5mV @ 1.5V)
- NMOS version for cost sensitive performance solutions.
- CMOS version for the designs requiring low power consumption
- NMOS Z0843004 - 4 MHz, Z0843006 - 6.17 MHz.
- CMOS Z84C3006 - DC to 6.17 MHz, Z84C3008 - DC to 8 MHz, Z84C3010 - DC to 10 MHz
- Interfaces directly to the Z80 CPU or—for baud rate generation—to the Z80 SIO.
- Standard Z80 Family daisy-chain interrupt structure provides fully vectored, prioritaized interrupts without external logic. The CTC may also be used as an interrupt controller.
- 6 MHz version supports 6.144 MHz CPU clock operation.

2) General description

The Z80 CTC, hereinafter referred to as Z80 CTC or CTC, four-channel counter/timer can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

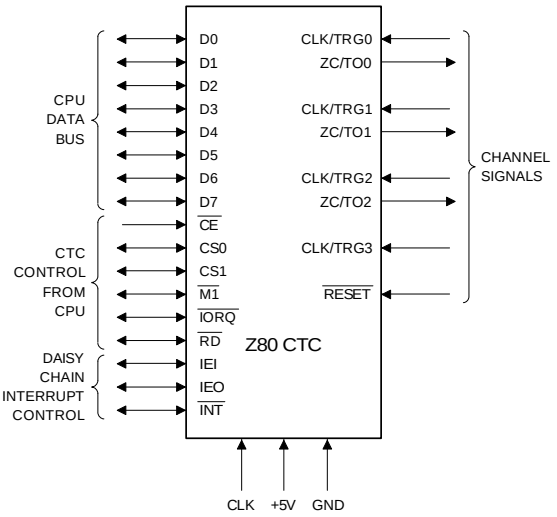


Figure 1. Pin Functions

Programming the CTC is straightforward: each channel is programmed with two bytes: a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified: the CTC internally generates a unique vector for each channel.

The Z80 CTC requires a single +5% V power supply and the standard Z80 single-phase system clock. It is packaged in 28-pin DIPs, a 44-pin plastic chip carrier, and a 44-pin Quad Flat Pack. (Figures 2a, 2b, and 2c). Note that the QFP package is only available for CMOS versions.

3) Pin configuration

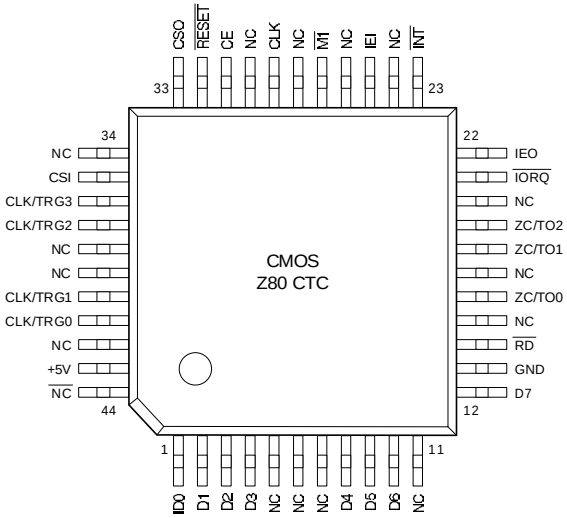


Figure 2c. 44-pin Quad Flat Pack Pin Assignments

4) Functional description

The Z80 CTC has four independent counter/timer channels. Each channel is individually programmed with two words: a control word and a time-constant word. The control word selects the operating mode (counter or timer), enables or disables the channel interrupt, and selects certain other operating parameters. If the timing mode is selected, the control word also sets a prescaler, which divides the system clock by either 16 or 256. The time-constant word is a value from 1 to 256.

During operation, the individual counter channel counts down from the preset time constant value. In counter mode operation the counter decrements on each of the CLK/TRG input pulses until zero count is reached. Each decrement is synchronized by the system clock. For counts greater than 256, more than one counter can be cascaded. At zero count, the down-counter is automatically reset with the time constant value.

The timer mode determines time intervals as small as 2 µs (8 MHz), 3 µs (6 MHz), or 4 µs (4 MHz) without additional logic or software timing loops. Time intervals are generated by dividing the system clock with a prescaler that decrements a preset down-counter.

Thus, the time interval is an integral multiple of the clock period, the prescaler value (16 or 256), and the time constant that is preset in the down-counter. A timer is triggered automatically when its time constant value is programmed, or by an external CLK/TRG input.

Three channels have two outputs that occur at zero count.

The first output is a zero-count/timeout pulse at the ZC/TO output. The fourth channel (Channel 3) does not have a ZC/TO output;interrupt request is the only output available from Channel 3.

The second output is Interrupt Request ($\overline{INT}$), which occurs if the channel has its interrupt enabled during programming. When the Z80 CPU acknowledges Interrupt Request, the Z80 CTC places an interrupt vector on the data bus.

The four channels of the Z80 CTC are fully prioritized and fit into four configuous slots in a standard Z80 daisy-chain interrupt structure. Channel 0 is the highest priority and Channel 3 the lowest. Interrupts can be individually enabled (or disabled) for each of the four channels.

5) Pin description

Pin No.	Symbol	Signal name	In/Out	Function
1	D0	S D0	In/Out	Data bus
2	D1	S D1	In/Out	Data bus
3	D2	S D2	In/Out	Data bus
4	D3	S D3	In/Out	Data bus
5	NC	NC	—	NC
6	NC	NC	—	NC
7	NC	NC	—	NC
8	D4	S D4	In/Out	Data busj*9
10	D6	S D6	In/Out	Data bus
11	NC	NC	—	NC
12	D7	S D7	In/Out	Data bus
13	GND	GND	—	GND
14	$\overline{RD}$	S $\overline{RDS}$	In	Read cycle status signal
15	NC	NC	—	NC
16	ZC/TO0	S TM0	Out	Zero count / Timeout signal
17	NC	NC	—	NC
18	ZC/TO1	NC	—	NC
19	ZC/TO2	NC	—	NC
20	NC	NC	—	NC
21	$\overline{IORQ}$	S IORQ	In	Input / Output request signal
22	IEO	NC	—	NC
23	$\overline{INT}$	S INT	Out	Interrupt request signal
24	NC	NC	—	NC
25	IEI	VCC	—	+5V
26	NC	NC	—	NC
27	$\overline{M1}$	S M1	In	Machine cycle one signal
28	NC	NC	—	NC
29	CLK	CLK	In	System clock
30	NC	NC	—	NC
31	$\overline{CE}$	S A6	In	Chip enable signal
32	$\overline{RESET}$	S $\overline{RES}$	In	Reset signal
33	CS0	S A0	In	Channelselect signal
34	NC	NC	—	NC

Pin No.	Symbol	Signal name	In/Out	Function
35	CS1	S A1	In	Channelselect signal
36	CLK/TRG3	S TM1	In	External clock / timer signal
37	CLK/TRG2	S TM0	In	External clock / timer signal
38	NC	NC	—	NC
39	NC	NC	—	NC
40	CLK/TRG1	S $\overline{\text{INTS}}$	In	External clock / timer signal
41	CLK/TRG0	VCC	In	+5V
42	NC	NC	—	NC
43	+5V	VCC	—	+5V
44	NC	NC	—	NC

2-6. μPD71037

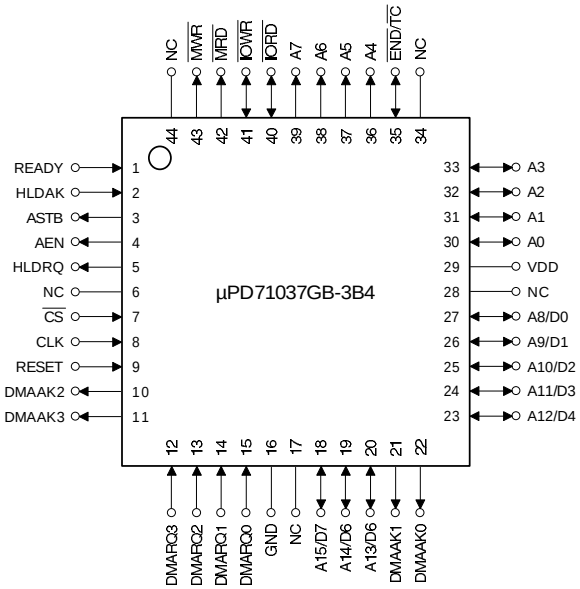
DMA CONTROLLER

The μPD71037 is a direct memory access controller (DMAC) for the micro processor system. It provides higher processing speed and lower power consumption in comparison with those in conventional use. Each of the four built-in DMA channels has 64-KB addresses and the function of counting the number of bytes of transferred data, and can transfer data from I/O to memory and from memory to memory as well.

1) FEATURES

- The clock speed is 10 MHz, twice that of the μPD8237A-5 (clock speed of 5 MHz).
- Each of the four DMA channels can be operated independently.
- Each channel can be self-initialized.
- Data is transferrable from memory to memory.
- Data in memory can independently initialized by block.
- High speed data transfer:
- 3.2 MB/sec. (clock seed of 10 MHz, normal transfer mode)
  5.0 MB/sec. (clock speed of 10 MHz, compression transfer mode)
- The number of DMA channels can directly be expanded (Expansion mode).
- $\overline{\text{END}}$ input when data transfer is finished.
- Software DMA request available.
- CMOS
- Low power consumption0

2) Pin configuration



3) Pin configuration

Pin No.	Symbol	Signal name	In/ Out	Function
1	READY	READY	In	Ready signal
2	HLDAK	HLDAK	In	Hold acknowledge signal
3	ASTB	S ASTB	Out	Address strobe signal
4	AEN	S AEN	Out	Address enable signal
5	HLDRQ	HLDRQ	Out	Hold request signal
6	NC	NC	—	NC
7	$\overline{\text{CS}}$	$\overline{\text{CS}}$	In	Chip select signal
8	CLK	CLK	In	Clock
9	RESET	SRNRESET	In	Reset signal
10	DMAAK2	S DACK2	Out	DMA acknowledge signal
11	DMAAK3	S DACK3	Out	DMA acknowledge signal
12	DMARQ3	S DRQ3	In	DMA request signal
13	DMARQ2	S DRQ2	In	DMA request signal
14	DMARQ1	S DRQ1	In	DMA request signal
15	DMARQ0	S DRQ0	In	DMA request signal
16	GND	GND	—	GND
17	NC	NC	—	NC
18	A15/D7	S D7	In/Out	Data bus
19	A14/D6	S D6	In/Out	Data bus
20	A13/D5	S D5	In/Out	Data bus
21	DMAAK1	S DACK1	Out	DMA acknowledge signal
22	DMAAK0	S DACK0	Out	DMA acknowledge signal
23	A12/D4	S D4	In/Out	Data bus
24	A11/D3	S D3	In/Out	Data bus
25	A10/D2	S D2	In/Out	Data bus
26	A9/D1	S D1	In/Out	Data bus
27	A8/D0	S D0	In/Out	Data bus
28	NC	NC	—	NC
29	VDD	VCC	—	+5V
30	A0	S A0	In	Address bus
31	A1	S A1	In	Address bus
32	A2	S A2	In	Address bus
33	A3	S A3	In	Address bus
34	NC	NC	—	NC
35	$\overline{\text{END}}$ / $\overline{\text{TC}}$	TC	In/Out	End / Terminal cut signal
36	A4	S A4	In	Address bus
37	A5	S A5	In	Address bus
38	A6	S A6	In	Address bus
39	A7	S A7	In	Address bus
40	$\overline{\text{IORD}}$	S $\overline{\text{IOR}}$	In/Out	I/O read signal
41	$\overline{\text{IOWR}}$	S $\overline{\text{IOW}}$	In/Out	I/O write signal
42	$\overline{\text{MRD}}$	S $\overline{\text{MRD}}$	Out	Memory read signal
43	$\overline{\text{MWR}}$	NC	—	NC
44	NC	NC	—	NC

2-7. MB62H149

1) Outline

The MB62H149 is a semi-custom LSI chip for the peripheral circuits in the SRN (SHARP Retail Network), its main function is to communicate data with the host CPU and control the peripheral circuits and transmission control circuits of the Sub CPU (Z-80). Fig. 2. shows the general configuration of the functions:

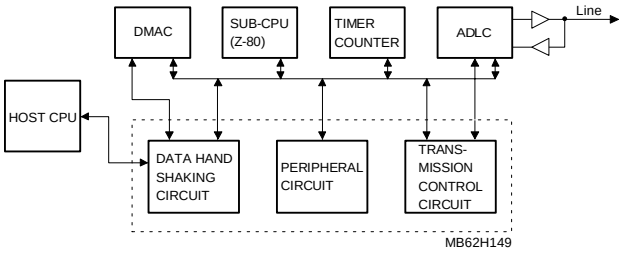


Fig. 2

2) Internal functions

(1) Data handshaking circuit

Is used because data processing speeds vary and the timing of the HOST CPU and SUB CPU do not synchronize, the MB62H149 is used for data handshaking. When the data handshaking portion is broken down, the system consists of a Write Signal from the HOST CPU to the MB62H149, Read Signal from the MB62H149 of the SUB CPU, Write Signal from the SUB CPU to the MB62H149 and Read Signal from the MB62H149 of the HOST CPU, all of which from two blocks as shown.

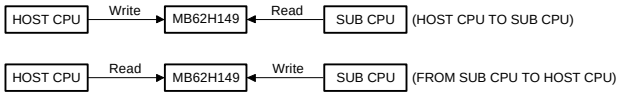


Fig. 3

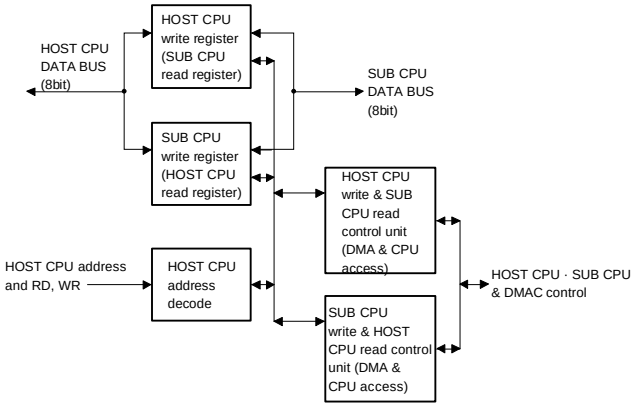

HOST CPU DATA BUS (8bit)
HOST CPU write register (SUB CPU read register)
SUB CPU DATA BUS (8bit)
SUB CPU write register (HOST CPU read register)
HOST CPU write & SUB CPU read control unit (DMA & CPU access)
HOST CPU address and RD, WR
HOST CPU address decode
HOST CPU · SUB CPU & DMAC control
SUB CPU write & HOST CPU read control unit (DMA & CPU access)

Fig. 4

(2) Peripheral circuit

The peripheral circuit consists of an I/O address generation unit on the SUB CPU, block dividing circuit, and the wait signal control unit.

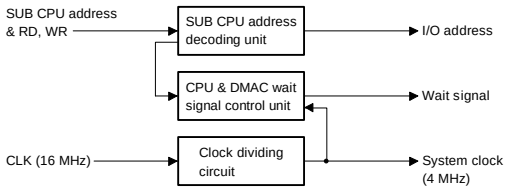

SUB CPU address & RD, WR
SUB CPU address decoding unit
I/O address
CPU & DMAC wait signal control unit
Wait signal
CLK (16 MHz)
Clock dividing circuit
System clock (4 MHz)

Fig. 5

(a) I/O address generation circuit

A total of 11 I/O addresses are generated by A0, A1, A4, A5 and RD and WR signals.

(b) CPU and DMAC wait signal control unit

Clocks into the CPU (Z-80), SUB CPU and its peripheral LSI, DMAC and CTC are operated respectively on 4 MHz.
While, the ADLC (MC68B54) (Advanced Data Link Control) is operated by the E (Enable clock) of 2 MHz according to restrictions in terms of the hardware of the LSI.
It is necessary to synchronize the timing of the write and read in the ADLC.
To control synchronization, timing, and input, the wait signal goes into the CPU for CPU access and into the DMAC for DMA access. This block is a circuit to generate such wait signal.

(c) Clock dividing circuit

This block divides the blocks according to the CLK supplied from outside to generate the clock for CPU, DMAC and CTC and the E and transmission clock rate (480 KBPS or 1 MBPS selectable) for the ADLC.

(3) Transmission control circuit

The transmission control circuit is divided into the modem unit, carrier detect unit, collision detect unit.

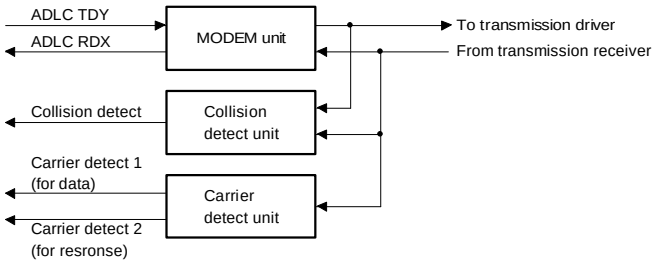


Fig. 6

(a) Modem circuit

The transmission data input from the ADLC are PE modulated (phase encoding modulation), the circuit to be output to the transmission driver and the reception data input from the transmission receiver are demodulated and produced at the ADLC.

(b) Collision detect circuit

The data transmitted from the home station is received and detects a collision on the transmission line by means of an exclusive OR gate.

(c) Carrier detect circuit

This circuit detects whether data is flowing on the transmission line. It consists of a circuit which immediately senses a no data status on the line. When data is not on the line the circuit functions to sense an elapse of the fixed time rate. The immediate sensing circuit is used for response testing and the delayed sensing circuit is used for data testing.
The fixed time rate is selectable according to the transmission speed as shown below via SRV-mode programming. Job #922.

Transmission speed	Delay time
1 MBPS	1.6m sec, 3.2m sec, 4.8m sec, 6.4m sec.
480 KBPS	3.2m sec, 6.4m sec, 9.6m sec, 12.8m sec.

3) Terminal Name and Description (MB62H149)

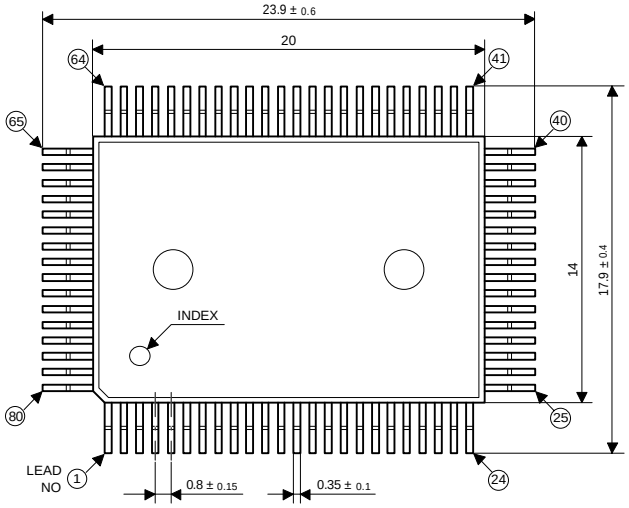
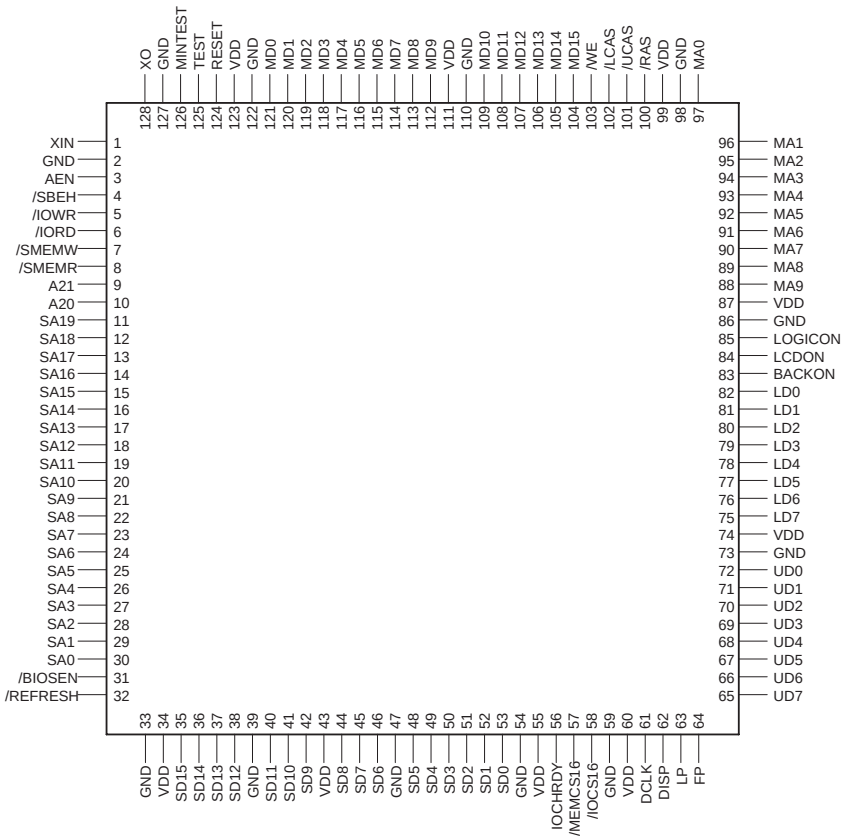


Fig. 7

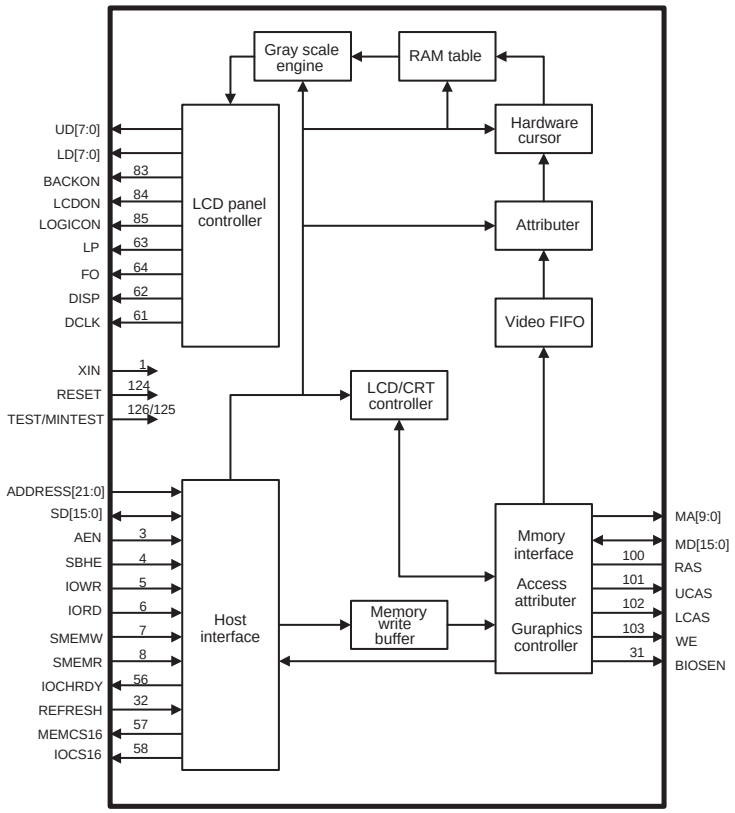
Pin No.	Terminal name	Host/ Sub	In/ Out	Description
1	CLK	Sub	In	Clock in (16 MHz)
2	—	—	—	N.U.
3	$\overline{\text{IORQ}}$	Sub	In	I/O request
4	$\overline{\text{MREQ}}$	Sub	In	Memory request
5	$\overline{\text{RDS}}$	Sub	In	Read from sub
6	$\overline{\text{WRS}}$	Sub	In	Write from sub
7	$\overline{\text{INTS}}$	Sub	Out	Interrupt to sub
8	ϕ	Sub	Out	Clock out
9	TM0	Sub	In	Timer 0
10	TM1	Sub	Out	Timer 1
11	$\overline{\text{MRD}}$	Sub	Out	Memory read
12	VSS	—	—	GND
13	$\overline{\text{WAIT}}$	Sub	Out	Wait signal
14	A15	Sub	Out	Address bus for DMA
16	A9	Sub	Out	
17	A8	Sub	Out	
18	A5	Sub	In	
19	A4	Sub	In	
20	A1	Sub	In	
21	A0	Sub	In	
22	DAK01	Sub	In	DMA acknowledge 0+1
23	—	—	—	N.U.
24	$\overline{\text{MWR0}}$	Sub	Out	Memory write
25	D7	Sub	I/O	Data bus
26	D6	Sub	I/O	
27	D5	Sub	I/O	
28	D4	Sub	I/O	
29	D3	Sub	I/O	
30	D2	Sub	I/O	
31	D1	Sub	I/O	
32	D0	Sub	I/O	
33	VDD	—	—	+5V
34	—	—	—	N.U.
35	$\overline{\text{RES}}$	Host	In	Reset
36	$\overline{\text{IO/WR}}$	Sub	I/O	I/O write
37	$\overline{\text{IO/RD}}$	Sub	I/O	I/O read
38	AEN	Sub	In	Address enable from DMAC
39	AST	Sub	In	Address strobe from DMAC
40	TCS	Sub	In	Terminal count
41	DAK23	Sub	In	DMA acknowledge 2+3
42	$\overline{\text{DRQRS}}$	Sub	Out	DMA request read to sub
43	$\overline{\text{DRQWS}}$	Sub	Out	DMA request write to sub
44	$\overline{\text{RDH}}$	Host	In	Read from Host
45	$\overline{\text{WRH}}$	Host	In	write from Host
46	$\overline{\text{INTH}}$	Host	Out	Interrupt to host
47	$\overline{\text{DAK}}$	Host	In	DMA acknowledge from host
48	TCH	Host	In	Terminal count from host
49	$\overline{\text{DRQWH}}$	Host	Out	DMA request read to host
50	$\overline{\text{DRQWH}}$	Host	Out	DMA request write to host
51	$\overline{\text{CS}}$	Host	In	Chip select from host
52	VSS	—	—	GND
53	—	—	—	N.U.
54	DB0	Host	I/O	Data bus
55	DB1	Host	I/O	Data bus
56	DB2	Host	I/O	Data bus
57	DB3	Host	I/O	Data bus
58	DB4	Host	I/O	Data bus
59	DB5	Host	I/O	Data bus
60	DB6	Host	I/O	Data bus
61	DB7	Host	I/O	Data bus
62	AB0	Host	In	Address bus from host
63	—	—	—	N.U.
64	AB1	Host	In	Address bus from host
65	COL	Sub	In	Collision detect signal
66	RDI	Sub	In	Receive data from receiver
67	TDI	Sub	Out	Transmmit data to driver
68	$\overline{\text{RTS}}$	Sub	In	Request to send
69	RXC	Sub	Out	Receive clock to ADLC
70	RXD	Sub	Out	Receive data to ADLC
71	TXC	Sub	Out	Transmmit clock
72	TXD	Sub	In	Transmmit data
73	VDD	—	—	+5V
74	E	Sub	In	Enable clock to ADLC
75	$\overline{\text{IRQ}}$	Sub	In	Interrupt request from ADLC
76	$\overline{\text{LCS}}$	Sub	Out	Link controller chip select
77	—	—	—	N.U.
78	RS1	Sub	Out	Register select 1
79	RS0	Sub	Out	Register select 0
80	MSK	Sub	Out	Mask signal

2-8. VGA controller (MN89303A)

1) Pin Configuration



2) Block diagram



3) Pin configuration

Pin No.	Symbol	Signal name	In/ Out	Function
1	XIN	XIN	In	25.175MHz
2	GND	GND	In	GND
3	AEN	GND	In	GND
4	/SBEH	/SBEH	In	System byte high enable
5	/IOWR	/IOWR	In	I/O write
6	/IORD	/IORD	In	I/O read
7	/SMEMW	/SMEMW	In	Meory write
8	/SMEMR	/SMEMR	In	Memory read
9	A21	GND	In	GND
10	A20	GND	In	GND
11	SA19	VCC	In	+5V
12	SA18	GND	In	GND
13	SA17	VCC	In	+5V
14	SA16	A16	In	Address bus
15	SA15	A15	In	Address bus
16	SA14	A14	In	Address bus
17	SA13	A13	In	Address bus
18	SA12	A12	In	Address bus
19	SA11	A11	In	Address bus
20	SA10	A10	In	Address bus
21	SA9	A9	In	Address bus
22	SA8	A8	In	Address bus
23	SA7	A7	In	Address bus
24	SA6	A6	In	Address bus
25	SA5	A5	In	Address bus
26	SA4	A4	In	Address bus
27	SA3	A3	In	Address bus
28	SA2	A2	In	Address bus
29	SA1	A1	In	Address bus
30	SA0	A0	In	Address bus
31	/BIOSEN	NC	In	NC
32	/REFRESH	/RFSH	In	Refresh signal
33	GND	GND	In	GND
34	VDD	VCC	In	+5V
35	SD15	D7	I/O	Data bus
36	SD14	D6	I/O	Data bus
37	SD13	D5	I/O	Data bus
38	SD12	D4	I/O	Data bus
39	GND	GND	In	GND
40	SD11	D3	I/O	Data bus
41	SD10	D2	I/O	Data bus
42	SD9	D1	I/O	Data bus
43	VDD	VCC	In	+5V
44	SD8	D0	I/O	Data bus
45	SD7	D15	I/O	Data bus
46	SD6	D14	I/O	Data bus
47	GND	GND	In	GND
48	SD5	D13	I/O	Data bus
49	SD4	D12	I/O	Data bus
50	SD3	D11	I/O	Data bus
51	SD2	D10	I/O	Data bus
52	SD1	D9	I/O	Data bus
53	SD0	D8	I/O	Data bus
54	GND	GND	In	GND
55	VDD	VCC	In	+5V
56	IOCHRDY	/VWAITI	Out	Channel ready signal
57	/MEMCS16	NC	In	NC
58	/IOCS16	NC	In	NC
59	GND	GND	In	GND

Pin No.	Symbol	Signal name	In/ Out	Function
60	VDD	VCC	In	+5V
61	DCLK	XCK	Out	Data shift clock
62	DISP	DISP	Out	Display enable
63	LP	LP	Out	Line pulse
64	FP	YD	OUt	Frame pulse
65	UD7	DU7	Out	Upper data
66	UD6	DU6	Out	Upper data
67	UD5	DU5	Out	Upper data
68	UD4	DU4	Out	Upper data
69	UD3	DU3	Out	Upper data
70	UD2	DU2	Out	Upper data
71	UD1	DU1	Out	Upper data
72	UD0	DU0	Out	Upper data
73	GND	GND	In	GND
74	VDD	VCC	In	+5V
75	LD7	DL7	Out	Lower data
76	LD6	DL6	Out	Lower data
77	LD5	DL5	Out	Lower data
78	LD4	DL4	Out	Lower data
79	LD3	DL3	Out	Lower data
80	LD2	DL2	Out	Lower data
81	LD1	DL1	Out	Lower data
82	LD0	DL0	Out	Lower data
83	BACKON	BKLT	Out	Back light On
84	LCDON	LCDON	Out	LCD drive power on signal
85	LOGICON	NC	Out	LCD logic power on signal
86	GND	GND	In	GND
87	VDD	VCC	In	+5V
88	MA9	NC	Out	NC
89	MA8	MA8	Out	Memory address bus
90	MA7	MA7	Out	Memory address bus
91	MA6	MA6	Out	Memory address bus
92	MA5	MA5	Out	Memory address bus
93	MA4	MA4	Out	Memory address bus
92	MA3	MA3	Out	Memory address bus
91	MA2	MA2	Out	Memory address bus
92	MA5	MA5	Out	Memory address bus
93	MA4	MA4	Out	Memory address bus
94	MA3	MA3	Out	Memory address bus
95	MA2	MA2	Out	Memory address bus
96	MA1	MA1	Out	Memory address bus
97	MA0	MA0	Out	Memory address bus
98	GND	GND	In	GND
99	VDD	VCC	In	VCC
100	/RAS	/RASV	Out	RAS address strobe
101	/UCAS	/UCASV	Out	Upper CAS address strobe
102	/LCAS	/LCASV	Out	Lower CAS address strobe
103	/WE	/WEV	Out	Write enable
104	MD15	MD15	I/O	Memory data
105	MD14	MD14	I/O	Memory data
106	MD13	MD13	I/O	Memory data
107	MD12	MD12	I/O	Memory data
108	MD11	MD11	I/O	Memory data
109	MD10	MD10	I/O	Memory data
110	GND	GND	In	GND
111	VDD	VCC	In	+5V
112	MD9	MD9	I/O	Memory data
113	MD8	MD8	I/O	Memory data
114	MD7	MD7	I/O	Memory data

Pin No.	Symbol	Signal name	In/ Out	Function
115	MD6	MD6	I/O	Memory data
116	MD5	MD5	I/O	Memory data
117	MD4	MD4	I/O	Memory data
118	MD3	MD3	I/O	Memory data
119	MD2	MD2	I/O	Memory data
120	MD1	MD1	I/O	Memory data
121	MD0	MD0	I/O	Memory data
122	GND	GND	In	GND
123	VDD	VCC	In	+5V
124	RESET	RESET	In	Reset signal
125	MINTEST	GND	In	GND
126	TEST	GND	In	GND
127	GND	GND	In	GND
128	XO	XO	Out	25.175MHz

2-9. CKDC9 (HD404728B02FS)

1) General description

The CKDC9 is a 4-bit microcomputer developed for the ER-A770 and provides functions to control the real-time clock, keys, and displays. The basic functions of the CKDC7 are shown below.

Keys: The CKDC9 is capable of controlling a maximum of 256 momentary keys. (Sharp 2-key rollover control)
Simultaneous scanning of key and switch
(When a key is scanned, the state of a mode and clerk switch is also buffered. The host can scan the state of switch together with the key entry data at the same time the key is scanned.)

Switches: Mode switch with 14 positions maximum
8-bit clerk (cashier) switch
2-bit feed switch
1-bit receipt on/off switch
1-bit option switch
4-bit general-purpose switch (1-bit is used for keyboard select)

Displays: 16-column dot display
12-column 7-segment display (column digit selectable)
All column blink controlled for the dot and 7-segment display decimal point and indicators
Programmable patterns for 7-segment display:
Four patterns
Internal driver for 7-segment display

Buzzer: Single tone control

Clock: Year, month, day of month, day of week, hour, minute

Alarm: Hour, minute

Interrupt request (event control):

Detection of key input, switch position change, alarm issue, and counter overflow

2) Pin description

Pin No.	Symbol	Signal name	In/ Out	Function
1	SB	SB	Out	Segment B
2	SC	SC	Out	Segment C
3	SD	SD	Out	Segment D
4	SE	SE	Out	Segment E
5	SF	SF	Out	Segment F
6	SG	SG	Out	Segment G
7	P4	AP	Out	
8	P0	NC	—	NC
9	P1	NC	—	NC
10	P2	DP	Out	Decimal point
11	P3	ID	Out	Indicator
12	$\overline{\text{MODR}}$	VCC	—	+5V
13	$\overline{\text{CFSR}}$	$\overline{\text{CFSR}}$	In	Clerk key, Feed key, Switch return signal
14	KEX0	NC	Out	NC
15	KEX1	NC	Out	NC
16	RQ	GND	—	GND
17	SKR0	VCC	—	+5V
18	ST0	ST0	Out	Key strobe signal
19	ST1	ST1	Out	Key strobe signal
20	ST2	ST2	Out	Key strobe signal
21	ST3	ST3	Out	Key strobe signal
22	$\overline{\text{POFF}}$	$\overline{\text{POFF}}$	In	Power off signal
23	$\overline{\text{STOP}}$	$\overline{\text{STOP}}$	In	STOP signal
24	$\overline{\text{DDIG}}$	VCC	—	+5V
25	$\overline{\text{DCS}}$	$\overline{\text{DCS}}$	—	Dot display controller chip select $\overline{\text{DCS}}$
26	VCC	$\overline{\text{VCKDC}}$	—	+5V
27	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$	In	Clock signal
28	HTS	HTS	In	Key data from host
29	STH	STH	Out	Key data to host
30	SDISP	GND	—	GND
31	BUZZ	BUZZ	Out	Buzzer
32	$\overline{\text{DSCK}}$	$\overline{\text{DSCK}}$	—	Dot display controller $\overline{\text{SCK}}$
33	$\overline{\text{SRES}}$	$\overline{\text{RESET}}$	Out	Reset signal
34	DS0	$\overline{\text{DSO}}$	—	Dot display controller SO
35	$\overline{\text{SHEN}}$	$\overline{\text{SHEN}}$	Out	Shift enable signal
36	$\overline{\text{IRQ}}$	$\overline{\text{KRQ}}$	Out	Key request signal
37	KR0	$\overline{\text{KR0}}$	In	Key return signal
38	KR1	$\overline{\text{KR1}}$	In	Key return signal
39	KR2	$\overline{\text{KR2}}$	In	Key return signal
40	KR3	$\overline{\text{KR3}}$	In	Key return signal
41	RESET	CKDCR	In	CKDC reset signal
42	OSC2	OSC2	—	Clock
43	OSC1	OSC1	—	Clock
44	GND	GND	—	GND
45	CL1	CL1	—	Time clock
46	CL2	CL2	—	Time clock
47	TEST	VCKDC	—	+5V
48	G0	G1	Out	Display digit signal
49	G1	G2	Out	Display digit signal
50	G2	G3	Out	Display digit signal
51	G3	G4	Out	Display digit signal
52	G4	G5	Out	Display digit signal
53	G5	G6	Out	Display digit signal
54	G6	G7	Out	Display digit signal
55	G7	G8	Out	Display digit signal
56	G8	G9	Out	Display digit signal
57	G9	G10	Out	Display digit signal
58	G10	G11	Out	Display digit signal
59	G11	NC	Out	NC
60	PO0	NC		NC
61	PO1	NC		NC
62	PO2	NC	—	NC
63	PO3	NC	—	NC
64	SA	SA	—	Segment A

2-10. ISP2032

This IC has been developed specially for UP-3300 to achieve VGA CHIP and PSRAM interfaces.

Pin descriotion

Pin No.	Name	I/O	Function
1	/VMEM	In	VIDEO MEMORY DECODE C00000H ~ C1FFFFH 16bit/8bit access, 8 bit read from the CPU is treated as 16-bit on the VGA.
2	/VMEM2	In	VIDEO MEMORY DECODE (ONLY FOR GRAPHICS MODE; 8BIT) C80000H ~ C9FFFFH 8-bit access only. /VMEM and /VMEM2 differ in their apparent address to each other, but the contents of memory to be accessed are the same. They differ in access method (WORD/BYTE).
3	/HWR	In	HIGH BYTE WRITE FROM CPU
4	/LWR	In	LOW BYTE WRITE FROM CPU
5	PHAI	In	CLOCK FROM CPU
6	VCC		
7	/ISPEN	In	for ISP (In System Program)
8	/VWAITI	In	WAIT FROM VGA CHIP (IOCHRDY)
9	/VWAIT	Out	WAIT TO MPCA There are following 2 ORs. ① IOCHRDY from VGA CHIP ② 1 WAIT is generated when VRAM. VGA I/O is accessed. (Because IOCHRDY is slow, 1 WAIT is generated prior to it.)
10	/DWRI	In	DELAYED WRITE (FOR VGA CHIP TIMING)
11	/DWRO	Out	WRITE FOR /DWRI
12	/DRDI	In	DELAYED READ (FOR VGA CHIP TIMING)
13	/DRD	Out	READ FOR /PRDI
14	RES	Out	RESET OUTPUT RESET ← NOT (/RESET)
15	/RES	In	/RESET INPUT
16	A0	In	A0
17	GND		
18	A20	In	A20
19	PCE21E	Out	EXTENDED PSRAM1 DECODE (EVEN) 800000H ~ 8FFFFFH
20	PCE210	Out	EXTENDED PSRAM1 DECODE (ODD) 800000H ~ 8FFFFFH
21	PCE220	Out	EXTENDED PSRAM2 DECODE (ODD) 900000H ~ 9FFFFFH
22	PCE22E	Out	EXTENDED PSRAM2 DECODE (EVEN) 900000H ~ 9FFFFFH
23	/IPLON0	In	IPL SIGNAL
24	/PSRF0	Out	PSRAM REFRESH
25	/OWR	Out	PSRAM WRITE (ODD SIDE)
26	/M3SWP	Out	MODE3 BUS SWAP (FOR PSRAM ACCESS WHEN IPL)
27	Y2/SCLK		ISP
28	VCC		
29	Y1/RESET		ISP
30	MODE		ISP
31	RASPN2E	In	EXTENDED PSRAM2 DECODE (FROM MPCA) 800000H ~ 9FFFFFH
32	RASPN2	In	EXTENDED PSRAM2 DECODE (FROM MPCA) 800000H ~ 9FFFFFH
33	/RASPN12	In	PSRAM DECODE (FROM MPCA) 600000H ~ 9FFFFFH
34	/AS	In	/AS FROM CPU
35	/RD	In	/RD FROM CPU
36	/RFSH	In	/RFSH FROM CPU
37	/SMEMR	Out	VIDEO MEMORY READ (TO VGA CHIP)
38	/SMEMW	Out	VIDEO MEMORY WRITE (TO VGA CHIP)
39	GND		
40	/COE0		Not used
41	/IORD	Out	VGA IO READ (TO VGA CHIP)
42	/IOWR	Out	VGA IO WRITE (TO VGA CHIP)
43	/SBHE	Out	BUS HIGH ENABLE (TO VGA CHIP)
44	/VIO2	Out	VGA IO CHIP SELECT

3. Address map

3-1. Total memory space

The address map of the total memory space is shown below. As you can see, the memory space is divided into the following 5 blocks:

0page area (including the I/O area)

- VRAM
- RAM
- ROM
- Extended I/O area

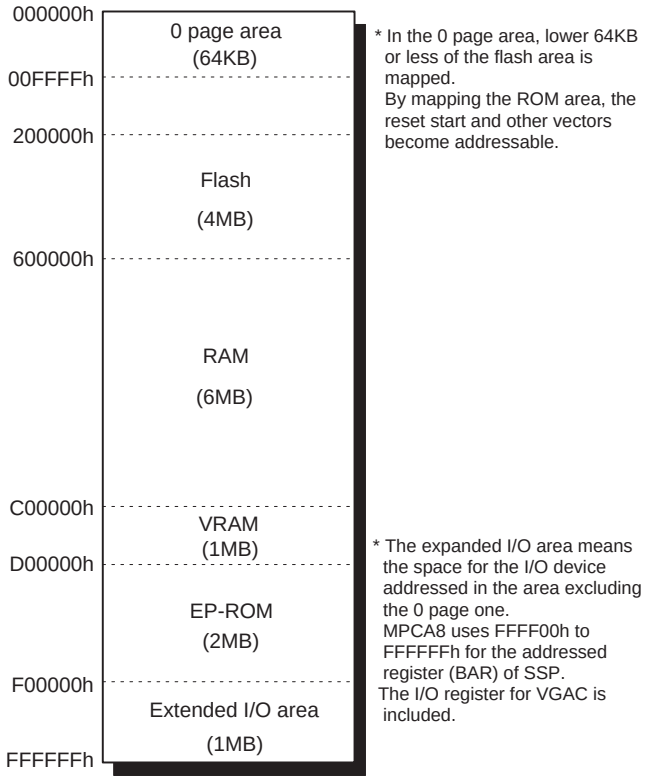


Fig. 2

3-2. 0page area

The 0page area consists of four spaces: the ROM mapped area, internal and external I/O areas.
The ROM mapped space have been devised for the following purposes:

① Simplifying the procedure for booting the IPL program

② Achieving high-speed accessing, and accessing by abbreviated instructions.

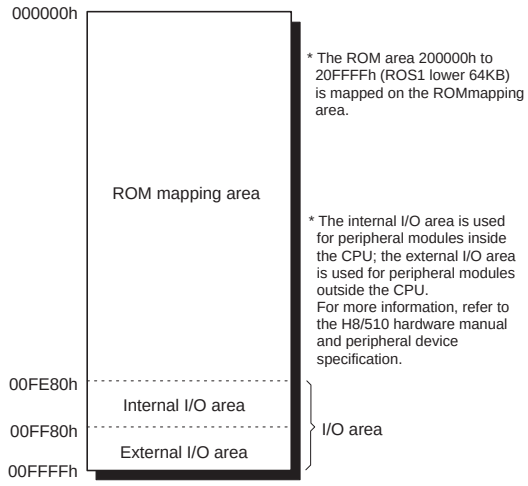

000000h
ROM mapping area
* The ROM area 200000h to 20FFFFh (ROS1 lower 64KB) is mapped on the ROMmapping area.
* The internal I/O area is used for peripheral modules inside the CPU; the external I/O area is used for peripheral modules outside the CPU.
For more information, refer to the H8/510 hardware manual and peripheral device specification.
00FE80h
Internal I/O area
00FF80h
External I/O area
00FFFFh
I/O area

Fig. 3

3-3. I/O areas

The addresses from 00FF80h to 00FFFFh are called the internal I/O area.
The internal I/O area is a space where the control registers and built-in ports inside the CPU are addressed.
The external I/O area is a space where the peripheral devices outside the CPU or devices on an optional card are addressed.

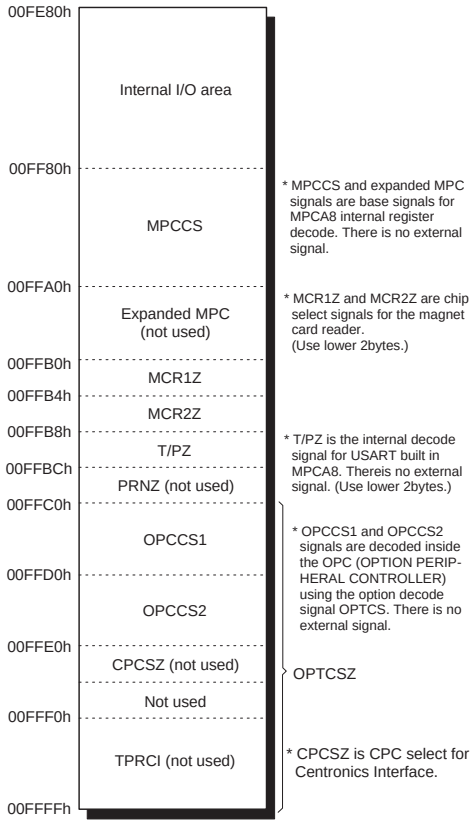

00FE80h
Internal I/O area
00FF80h
MPCCS
* MPCCS and expanded MPC signals are base signals for MPCA8 internal register decode. There is no external signal.
00FFA0h
Expanded MPC (not used)
* MCR1Z and MCR2Z are chip select signals for the magnet card reader. (Use lower 2bytes.)
00FFB0h
MCR1Z
00FFB4h
MCR2Z
00FFB8h
T/PZ
* T/PZ is the internal decode signal for USART built in MPCA8. Thereis no external signal. (Use lower 2bytes.)
00FFBCh
PRNZ (not used)
00FFC0h
OPCCS1
* OPCCS1 and OPCCS2 signals are decoded inside the OPC (OPTION PERIPHERAL CONTROLLER) using the option decode signal OPTCS. There is no external signal.
00FFD0h
OPCCS2
00FFE0h
CPCSZ (not used)
OPTCSZ
Not used
00FFF0h
TPRCI (not used)
* CPCSZ is CPC select for Centronics Interface.
00FFFFh

Fig. 4

3-4. ROM space

Fig.5 shows the ROM space. The ER-A770 uses 2MB of NOR-type flash memory instead of conventional ROM, so that the FROS1# from the MPCA8 is input into the chip enable of the flash memory.

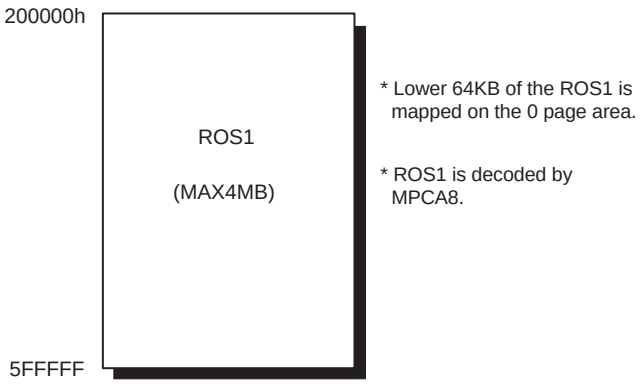


Fig. 5

3-5. VRAM & RAM space

The VRAM is the display memory of the LCD.

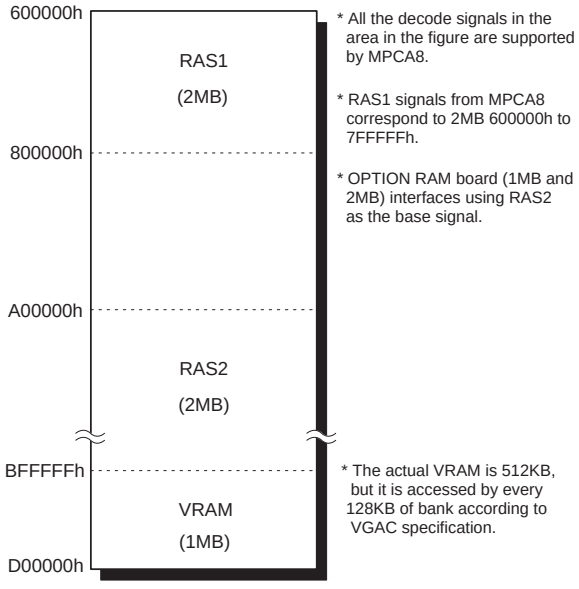

600000h
RAS1
(2MB)
* All the decode signals in the area in the figure are supported by MPCA8.
* RAS1 signals from MPCA8 correspond to 2MB 600000h to 7FFFFFh.
800000h
* OPTION RAM board (1MB and 2MB) interfaces using RAS2 as the base signal.
A00000h
RAS2
(2MB)
BFFFFFh
* The actual VRAM is 512KB, but it is accessed by every 128KB of bank according to VGAC specification.
VRAM
(1MB)
D00000h

Fig. 6

3-6. Extended I/O area

The addresses from F00000h to FFFFFFh are called an extended I/O area. The ER-A770 uses the following addresses as the break address register (BAR) for SSP.

- FFFF00h ~ FFFFFFh

4. LCD display

The ER-770 uses a 320 x 240 dot monochromatic LCD for the main display and VGAC (MN89303A) for the display controller which is connected to H8/510 in the ISA bus connection mode.

4-1. Block diagram

Here is the block diagram of the LCD and its allied components.

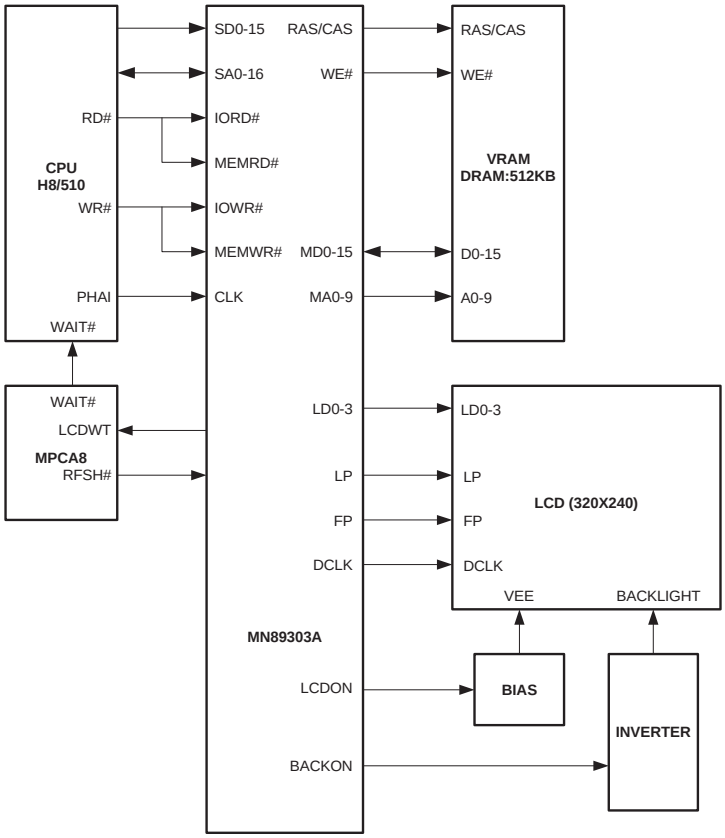


Fig. 7

4-2. LCD panel

The LCD panel uses a dot-matrix liquid crystal module LM320153 with monochromatic STN and COFT backlight. The resolution is 320 x 240.

4-3. Display controller

Matsushita VGAC (MN89303A) is used for display controller.

VRAM is on the address space of the CPU and data can be written on and read from it by every 128 KB of bank at the address C00000H ~ C1FFFFH from the CPU side. VRAM consists of 4 banks.

4-4. LCD ON control

The LCD's is bias power supply is controlled by the MN89303A terminal LCDON to turn the LCD screen on and off.

The LCDON is at "L" at resetting +5V power is supplied to the LCD by setting the expanded function control register bit5 of MN89303A to "H" with software. The LCD screen isn't turned on until +5V is supplied.

4-5. Back light control

The back light is turned ON/OFF by the MN89303A terminal BACKON. The initial value is "L" and the back light is off. By setting the expanded function control register bit6 of MN89303A to "H", the inverter unit is turned on.

4-6. Luminance and contrast adjustment

- Luminance: Luminance is adjusted with an inverter which has dimming function.
- Contrast: Contrast is adjusted by controlling the contrast adjustment voltage (VCON) of the LM320153

5. Customer display

The ER-770 can incorporate a UP-116DP (display tube unit for the UP-P16DP) for the customer display to carry out the same control as for the pole display (UP-P16DP).

6. Pseudo SRAM (Standard)

The device is TOSHIBA 4MB SRAM (TC51V8512AFT 512K 8bit) with access time of 120ns.

6-1. CPU interface

The figure below shows a typical pseudo SRAM interface in the ER-A770.

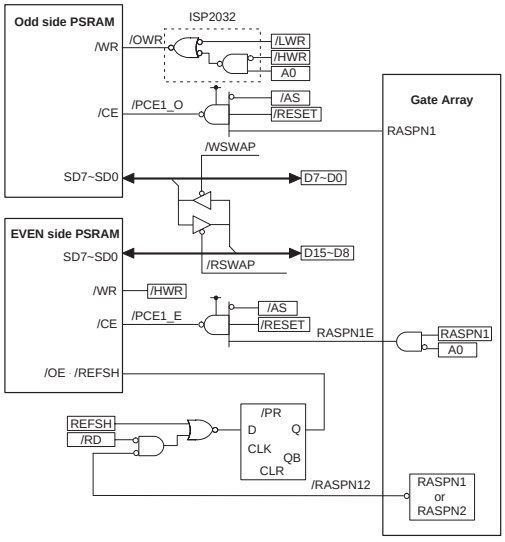


Fig. 8

6-2. Pseudo SRAM address

Standard SRAM is decoded as follows by the RASPN1 signal.

① 700000h ~ 7FFFFFh

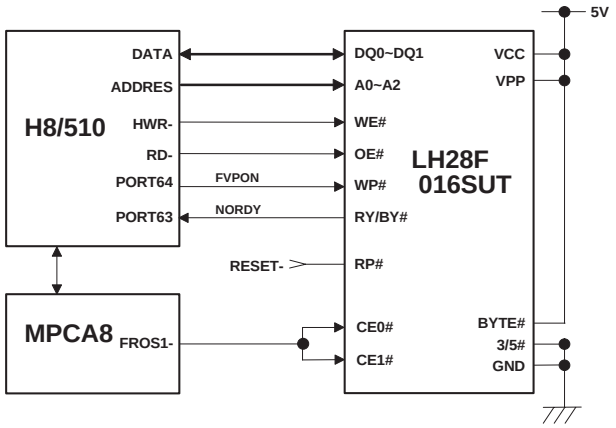
The base signal is 2MB. It thus wraparounds with 600000H ~ 6FFFFFH 1MB.
Pseudo SRAM consists of 1 chip for respective even and odd number addresses. Both of word and byte access from CPU are available.

7. NOR-type flash memory

Here is the explanation for the interface of NOR-type flash memory. The device is Sharp's LH28F016SU flash memory which consists of 512 K words × 16 or 1 MB × 8, with 32 blocks of 64 KB.

7-1. CPU interface

The figure below shows a typical interface for the LH28F016SU of the ER-A770 system.



7-2. Device control

After resetting, the device automatically enters the array read mode and perform the same action as the usual ROM, thus requiring no special consideration when reading data.

Data can be written at high speed by using the page buffer.

8. SSP control

The ER-A770 uses flash memory in the place of EPROM, so it is possible to rewrite the contents of the flash memory in changing the program. However, since the existing gate array MPCA8 is used, it is also possible to use the conventional SSP.

8-1. Operation

Like the MPCA7, the MPCA8 adopts the break address register comparison method for detecting addresses. The operation of this method is briefly explained below.

The gate array always compares the break address register (BAR) built in the gate array, with the address bus to monitor the address bus.

If both agree, the gate array outputs the NMI signal to the CPU, which in turn shifts from normal handling to exception handling.

In both the MPCA7 and the MPCA8, SSP is achieved by the above operation.

The setting of the break address register (BAR) is directly written in the addresses from FFFF00h to FFFFFFh.

9. Interrupt control

There are roughly two types of interrupts:

- Internal interrupts: Controlled inside the CPU
- External interrupts: Input into the CPU from outside

9-1. Internal interrupts

Device interrupts built in the CPU are used for the following applications:

Event factor		Application
SC11		Interrupt source as RS232 : CH8
SC12		Not used (SC1 is used for CKDC interface.)
FRT1	(ICI) (OCRA) (OCRB) (OVF)	INTMCR ~ MCR interrupt (to FT11 terminal)
FRT2	(ICI)	Standard SHEN event (for CKDC)
	(OCRA)	Simple IRC timer event
	(OCRB)	RS232 timer event
	(OVF)	System timer (53 ms)
TMR	(CMA) (CMB) (OVF)	
WDT	(OVF)	Drawer open timer
A/D		Not used
NMI		SSP request

9-2. External interrupts

The following types of external interrupts are available:

- $\overline{\text{NMI}}$ (SSP)
- $\overline{\text{IRQ0}}$ (Standard I/O interrupt)
- $\overline{\text{IRQ1}}$ (RS232 interrupt)
- $\overline{\text{IRQ2}}$ (Not Used)
- $\overline{\text{IRQ3}}$ (Used as SCK terminal)

10. WAIT control

The weight control function built in the MPCA8 is used to provide an interface with low-speed devices.

10-1. Block diagram

The block diagram of the wait control function is shown.

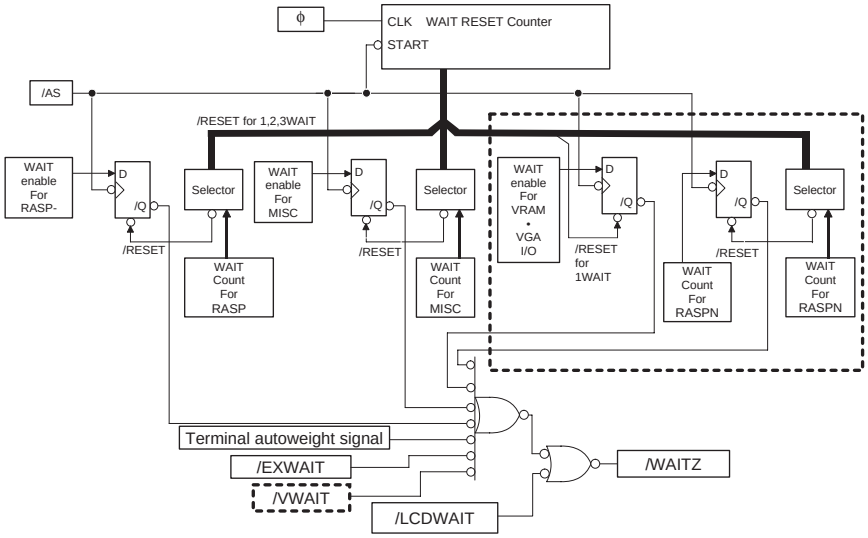


Fig. 10

In the figure, the decoder, wait enabling register, AND-OR sections are the same as those in the MPCA6 or 7, but other components are newly incorporated in the MPCA7.

EXWAITZ and WAITZ are external weight signals which are to be ORed inside the MPCA8 and output to the WAITZ. The EXWAITZ is a general-purpose wait request terminal, and WAITZ is the wait request signal from the VGA controller.

11. CKDC9

The ER-A770 on CKDC9 for the CKDC PWB and one CKDC9 for POLE display (option) to carry out the following control operations.

CKDC PWB CKDC9:

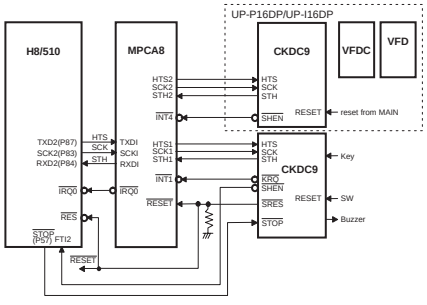
- Clock (second data readable)
- Buzzer
- System reset
- Key/Clerk switch

POLE CKDC9(UP-P16DP or UP-I16DP)

- Customer display tube

11-1. Interface

CKDC9 is connected through the MPCA8.



12. Option RAM interface

12-1. Interface

The expanded RAM connector terminals are shown in the table.

The 72 pin S.O. DIMM is used for the connector.

Extension RAM connector terminals

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	1	—	25	D9	49
GND	2	—	26	D8	50
—	3	—	27	D7	51
—	4	—	28	D6	52
—	5	A13	29	D5	53
—	6	A12	30	D4	54
—	7	A11	31	D3	55
—	8	A10	32	D2	56
—	9	A9	33	D1	57
—	10	A8	34	D0	58
A14	11	A7	35	GND	59
A15	12	A6	36	NC	60
A16	13	A5	37	$\overline{OWR}$	61
A17	14	A4	38	—	62
A18	15	A3	39	—	63
A19	16	A2	40	—	64
—	17	A1	41	—	65
$\overline{PCE22\_E}$	18	A0	42	—	66
$\overline{PCE21\_E}$	19	D15	43	$\overline{HWR}$	67
—	20	D14	44	—	68
$\overline{PSREF}$	21	D13	45	VMEM	69
$\overline{PCE22\_O}$	22	D12	46	VMEM	70
$\overline{PCE21\_O}$	23	D11	47	GND	71
GND	24	D10	48	GND	72

13. Reset sequence

The reset sequence block diagram is shown below. Note that $\overline{\text{RESET}}$ signal (system reset) and $\overline{\text{CKDCR}}$ signal (CKDC reset) are different from each other.

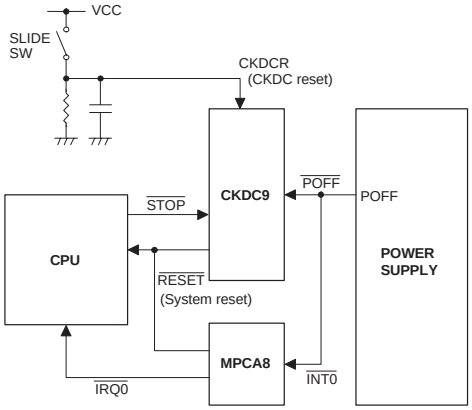


Fig. 14

13-1. Power ON/OFF

The flow of signal processing at the time of the power supply turning On/Off is as follows:

Table 19

<Power OFF>

	Power supply	MPCA8	CPU	CKDC9
1	$\overline{\text{POFF}}$ → L			
2		$\overline{\text{IRQ0}}$ → L		
3			$\overline{\text{STOP}}$ → L	
4				$\overline{\text{RESET}}$ → L (System reset)

Table 20

<Power ON>

	Power supply	MPCA8	CPU	CKDC9
1	$\overline{\text{POFF}}$ → H			
2				$\overline{\text{RESET}}$ → H (System reset)

The table below shows the timing chart.

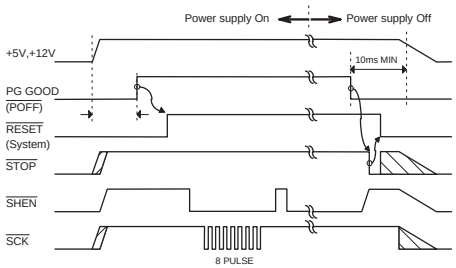


Fig. 15

13-2. MRS, SRV reset

The ER-A770 does not have the mode switch. The procedure for resetting MRS, SRV is different from that of conventional cash registers.

in the ER-A770, MRS, SRV resetting is selected and executed by the key which has bee depressed when the CKDC reset is released to start the system.

(In the case of MRS, security is added by a key operation equivalent to a pass word.)

Flow chart

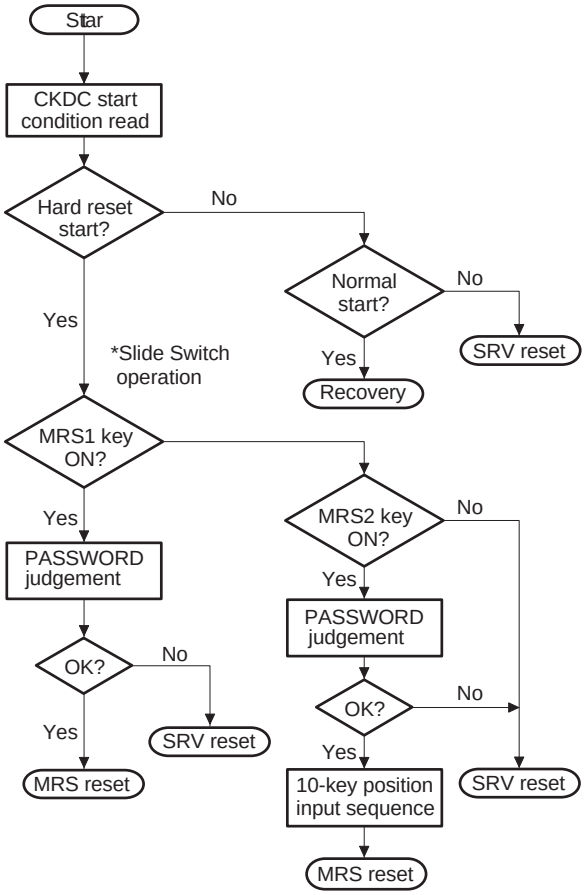


Fig. 16

14. Drawer

The ER-A770 can use up to 2 optional external drawers.

14-1. Drawer solenoid drive

P34 ~ P37 inside the CPU are allocated for the port output of the drawer solenoid drive.

Built-in port	Signal name	Remarks
P34	$\overline{\text{DR0}}$	Drawer 1 (optional drawer)
P35	$\overline{\text{DR1}}$	Drawer 2 (optional drawer)
P36	$\overline{\text{DR2}}$	Reserved
P37	$\overline{\text{DR3}}$	Reserved

One port corresponds to one drawer. Theoretically, it is possible to drive multiple drawers at the same time, but this processing must be inhibited softwarewisely because of power supply capacity and driver hardware factors. If a power failure is detected, the drawer solenoid drive must be stopped as soon as possible.

∗ The drawer solenoid drive time must controlled in the range of 40 ms to 50 ms by the timer.

14-2. Drawer open/close sense

The drawer open/close sense signal is input into the built-in port of the CPU. the sense signal of an optional drawer sensor is also wired ORed before inputting.

- P33=1: Any of the drawers is open.

15. SRN

The SRN of the ER-A770 is compatible with the ER-A750.

16. RS232

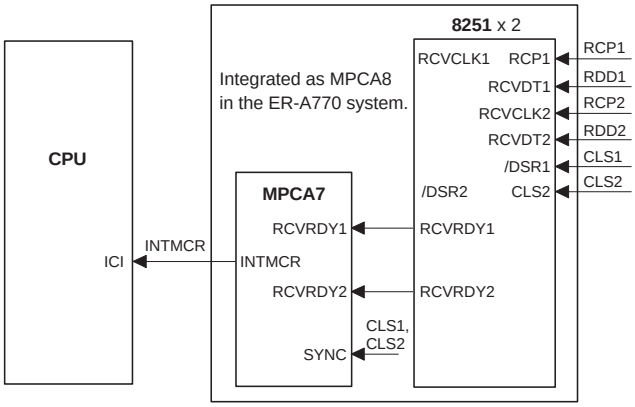
Two standard RS232 channels are compatible with the ER-A5RS. However, while the ER-A5RS uses the $\overline{IRQ2}$ terminal of the CPU for interruption of the RS232, the ER-A770 cannot use the $\overline{IRQ1}$ terminal instead of it. (The $\overline{IRQ2}$ terminal is used for IR as the SCK1 terminal.)
The standard RS232 is fixed to the logic channels 1 and 8. Use the channels 2, 3, 4, 5 and 6 for the ER-A7RS.

17. MCR

This paragraph describes MCR option (UP-E12MR) control defined by ER-A770 hardware architecture.
2 channels of the serial port (interchangeable with 8251) built in the MPCA8 are used. 2 tracks of data are read simultaneously. Supports the first and second tracks MCR of ISO. (UP-E12MR)

17-1. CPU interface

The CPU interface for the USART (8251) and magnet card reader (MCM-21) in the ER-A770 system is shown below.



Signal description

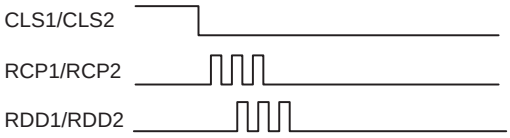
RCP1	TRACK 1 CLOCK PULSE
RDD1	TRACK 1 DATA SIGNAL
RCP2	TRACK 2 CLOCK PULSE
RDD2	TRACK 2 DATA SIGNAL
CLS1	TRACK 1 CARD DETECTION SIGNAL
CLS2	TRACK 2 CARD DETECTION SIGNAL
RCVRDY1	TRACK 1 DATA RECEIVING SIGNAL
RCVRDY2	TRACK 2 DATA RECEIVING SIGNAL
INTMCR	INTERRUPT SIGNAL OR-SYNTHESIZED from RCVRDY and SYNC input

2 chip select signals for 8251 are generated inside MPCA8.

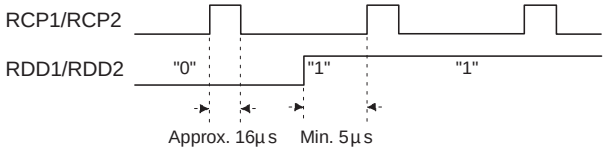
17-2. MCR interface

The operating timing of the MCR interface signals is given below.

(1) Example of timing



(2) Detailed timing (relation between DATA and CLOCK PULSE)

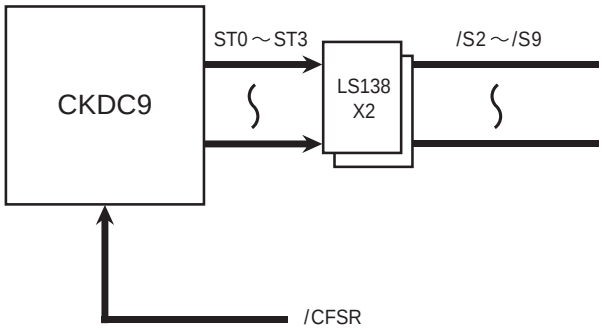


The "NULL" CODE is basically written prior to the opening code. The opening code detection algorithm is considered because data may become corrupt before and after the CARD detection signal due to a worn magnet stripe.

18. 1-HOLE CLERK

On the ER-A770, 1-hole clerk key with up to 8 bits can be used.

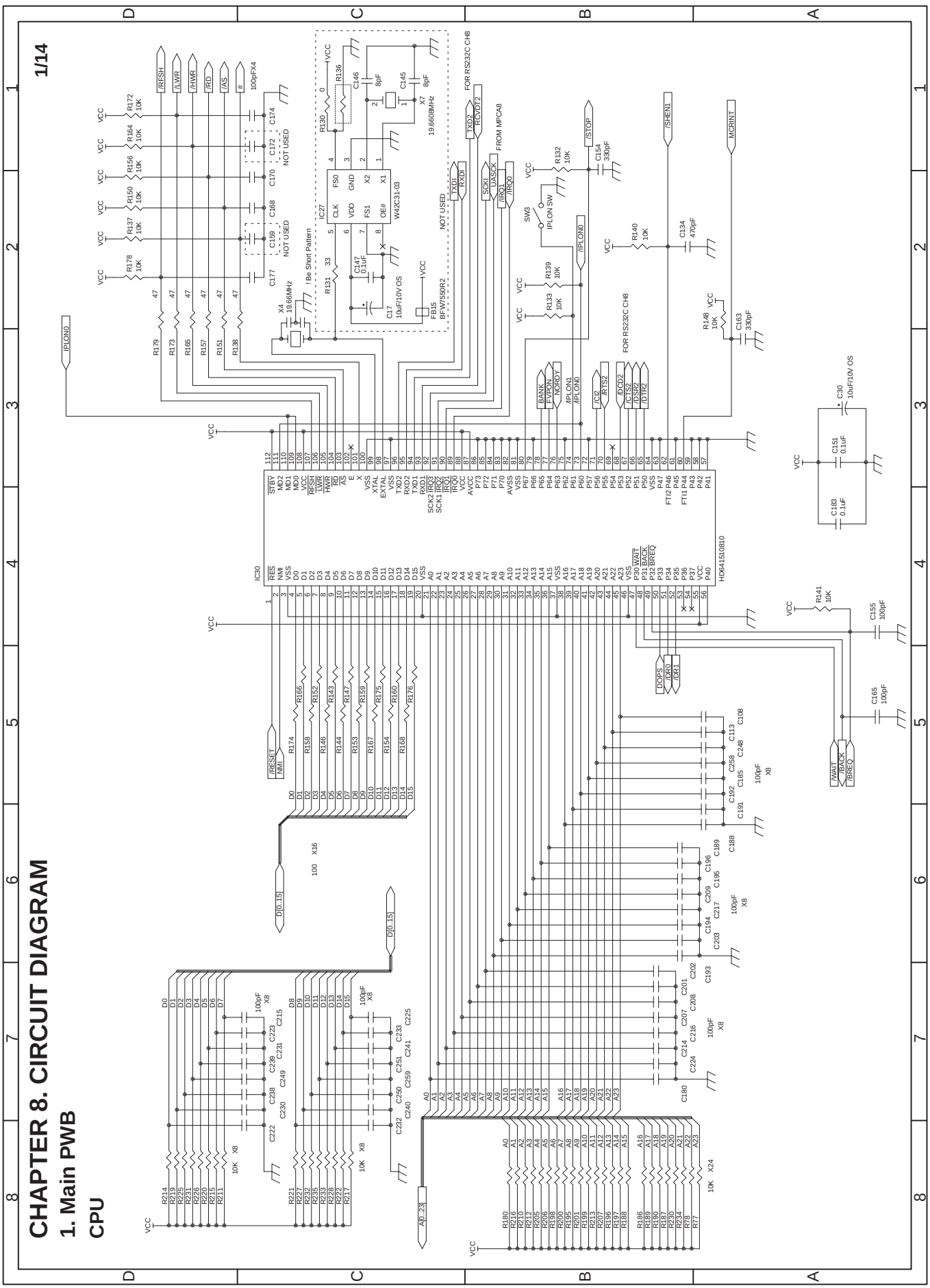
The 1-hole clerk switch is controlled through the CKDC9 on the main board.

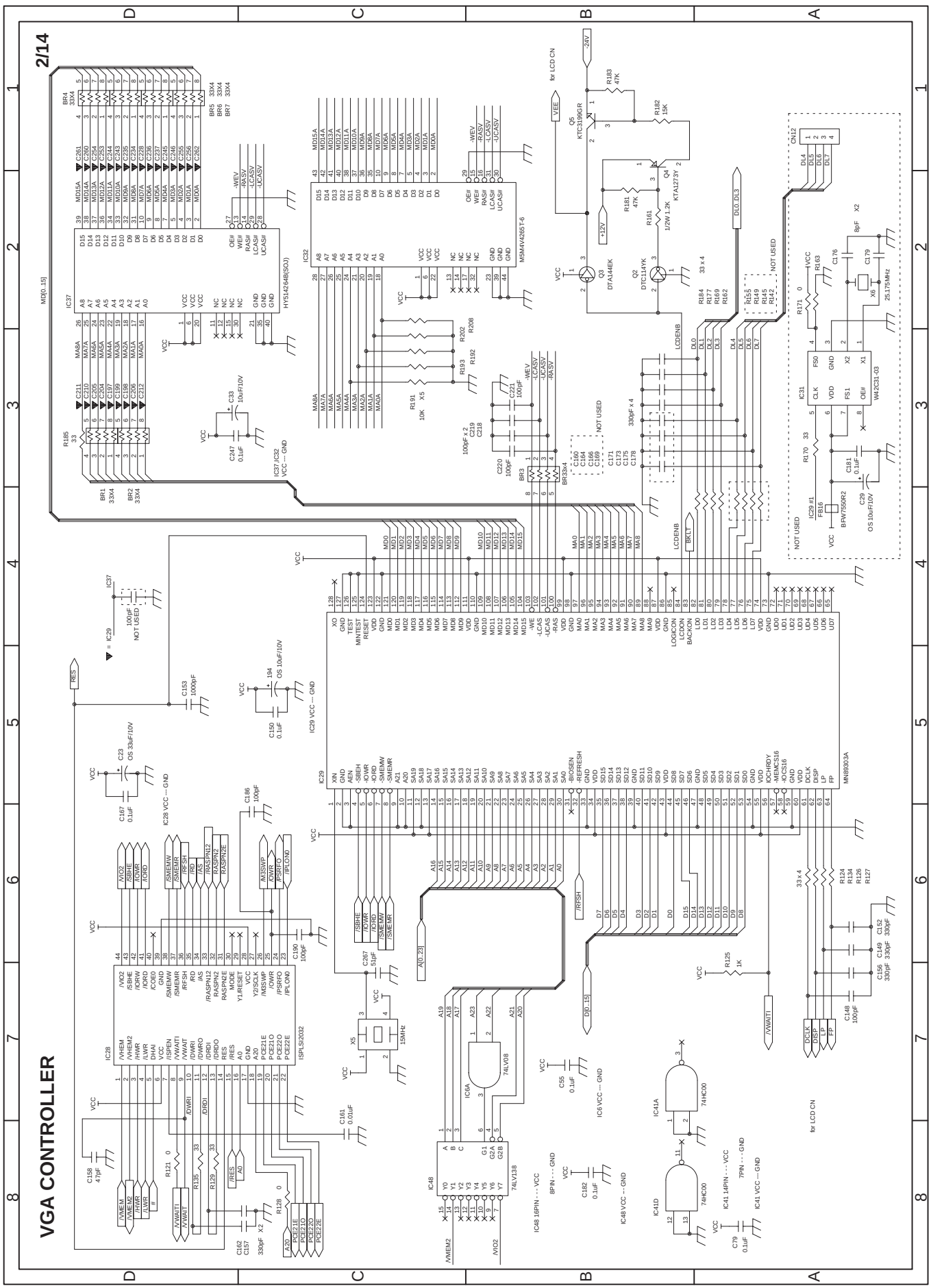


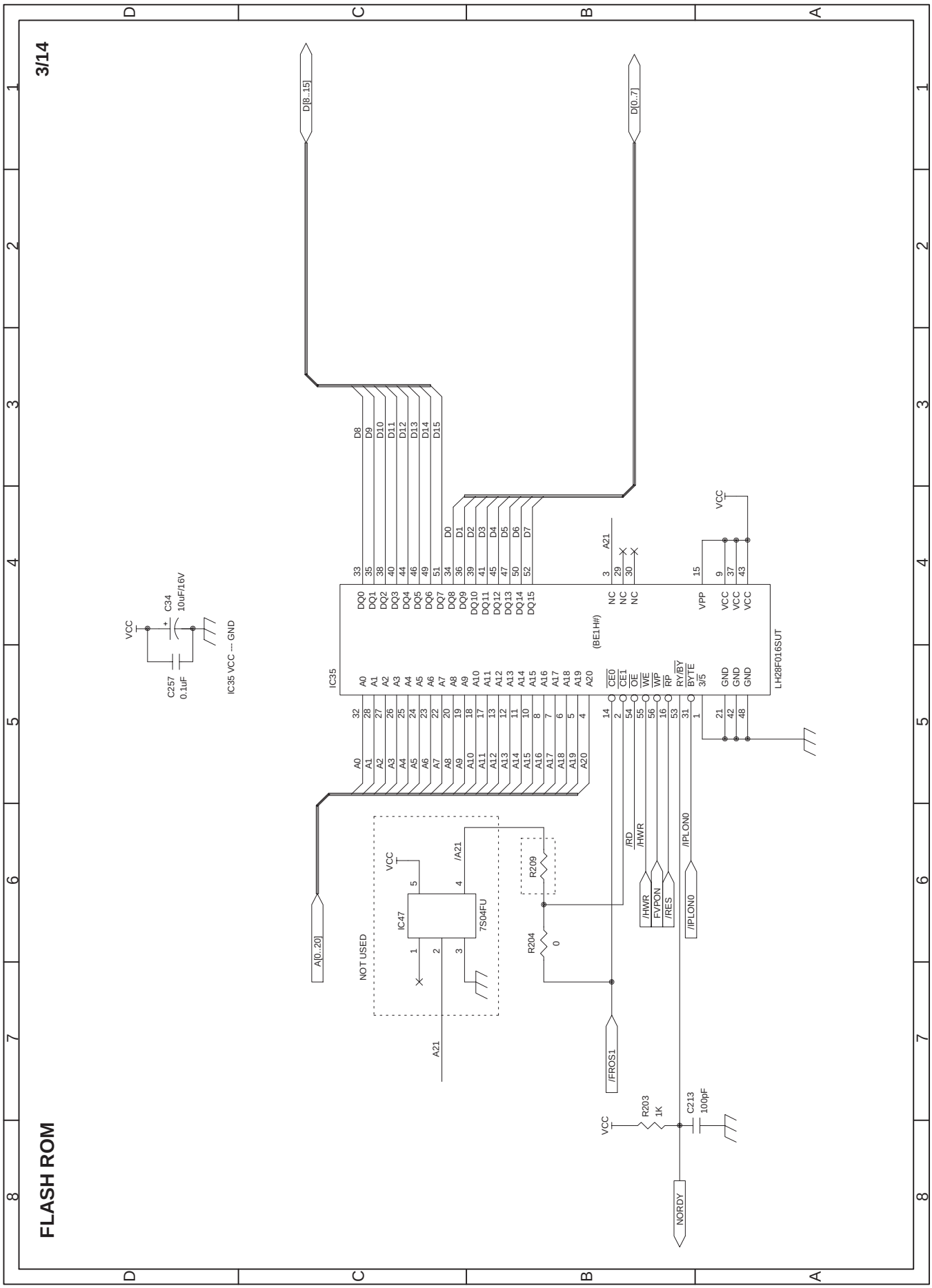
CHAPTER 8. CIRCUIT DIAGRAM

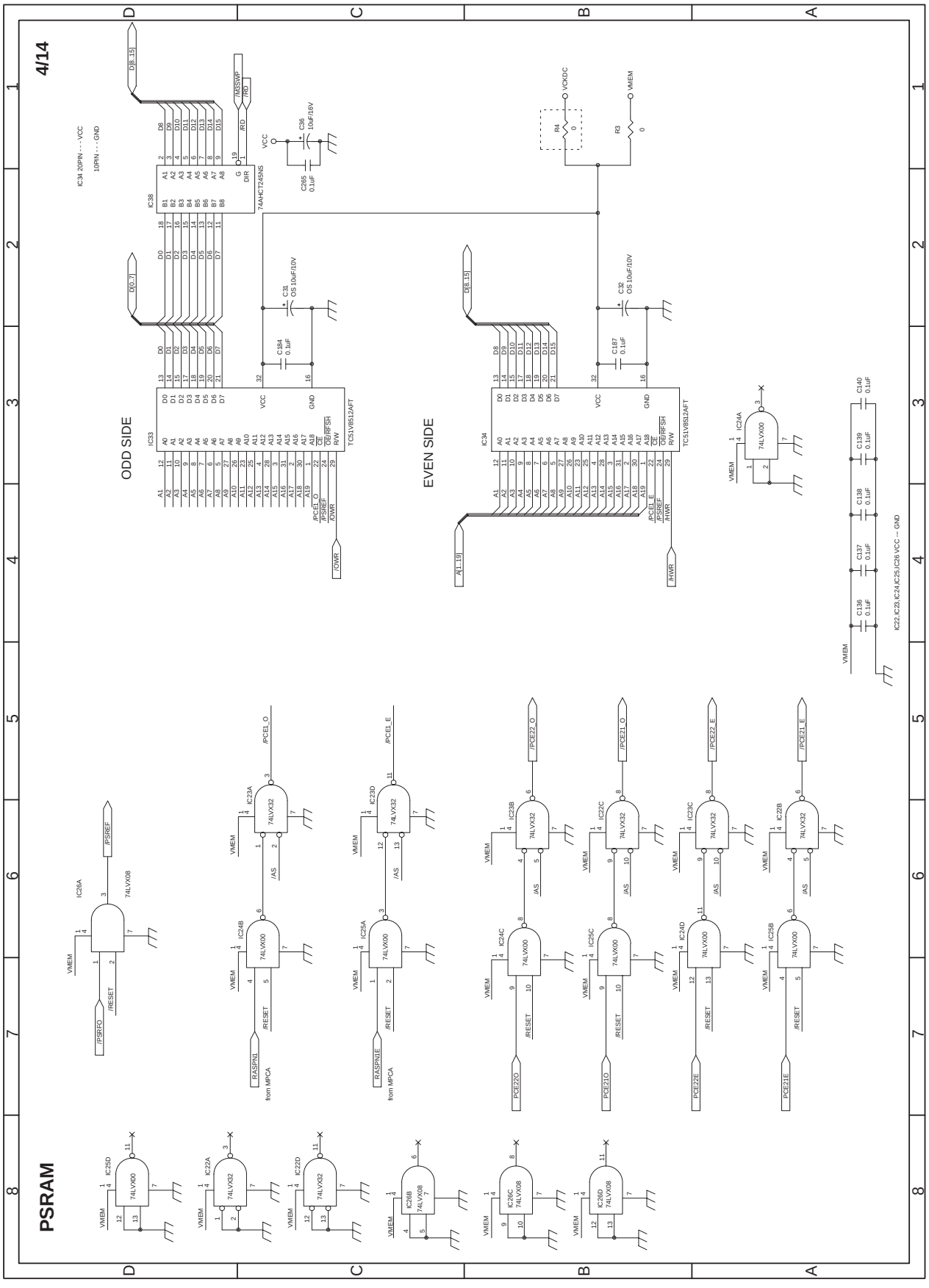
1. Main PWB

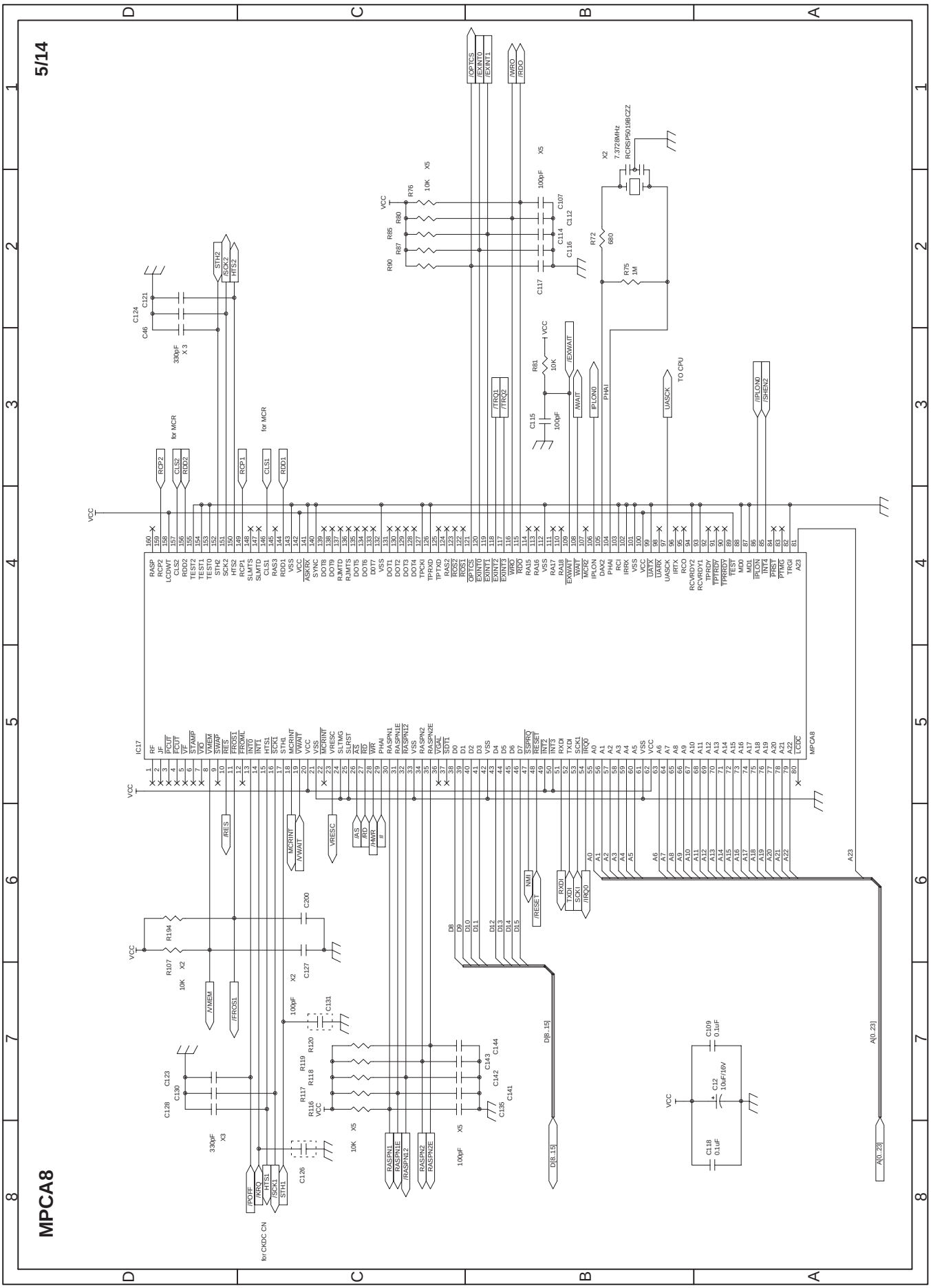
CPU

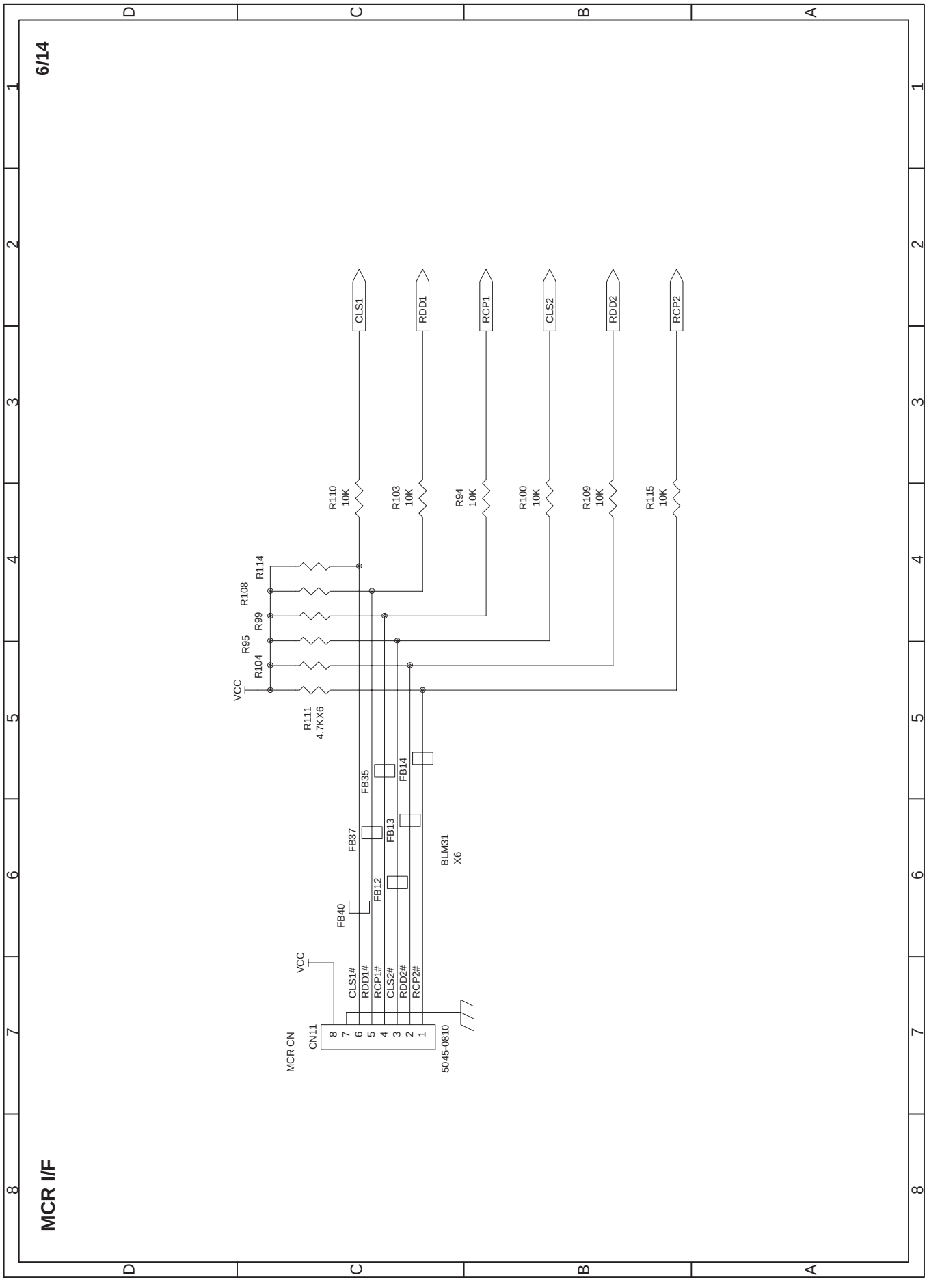


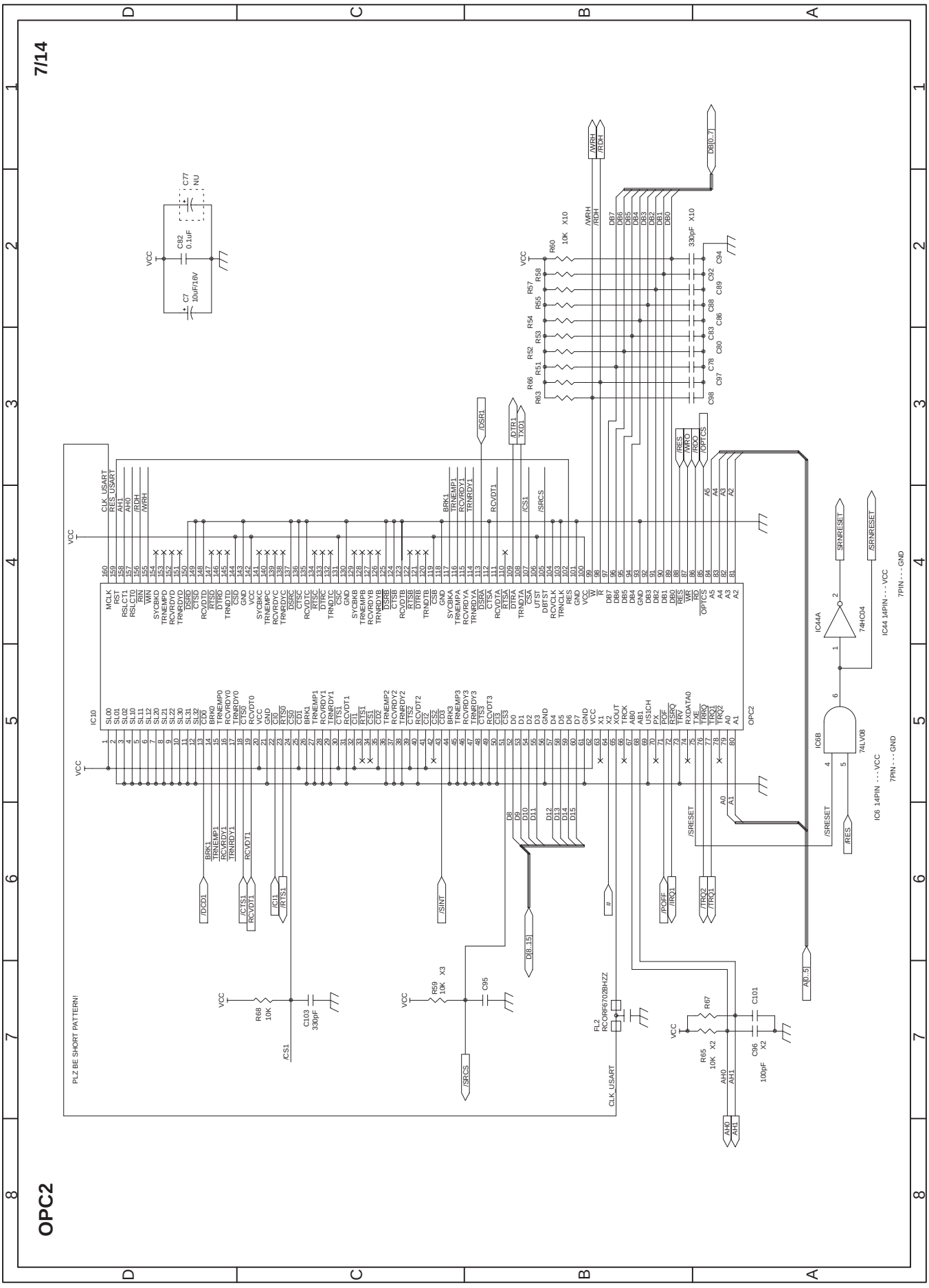

VGA CONTROLLER
2/14

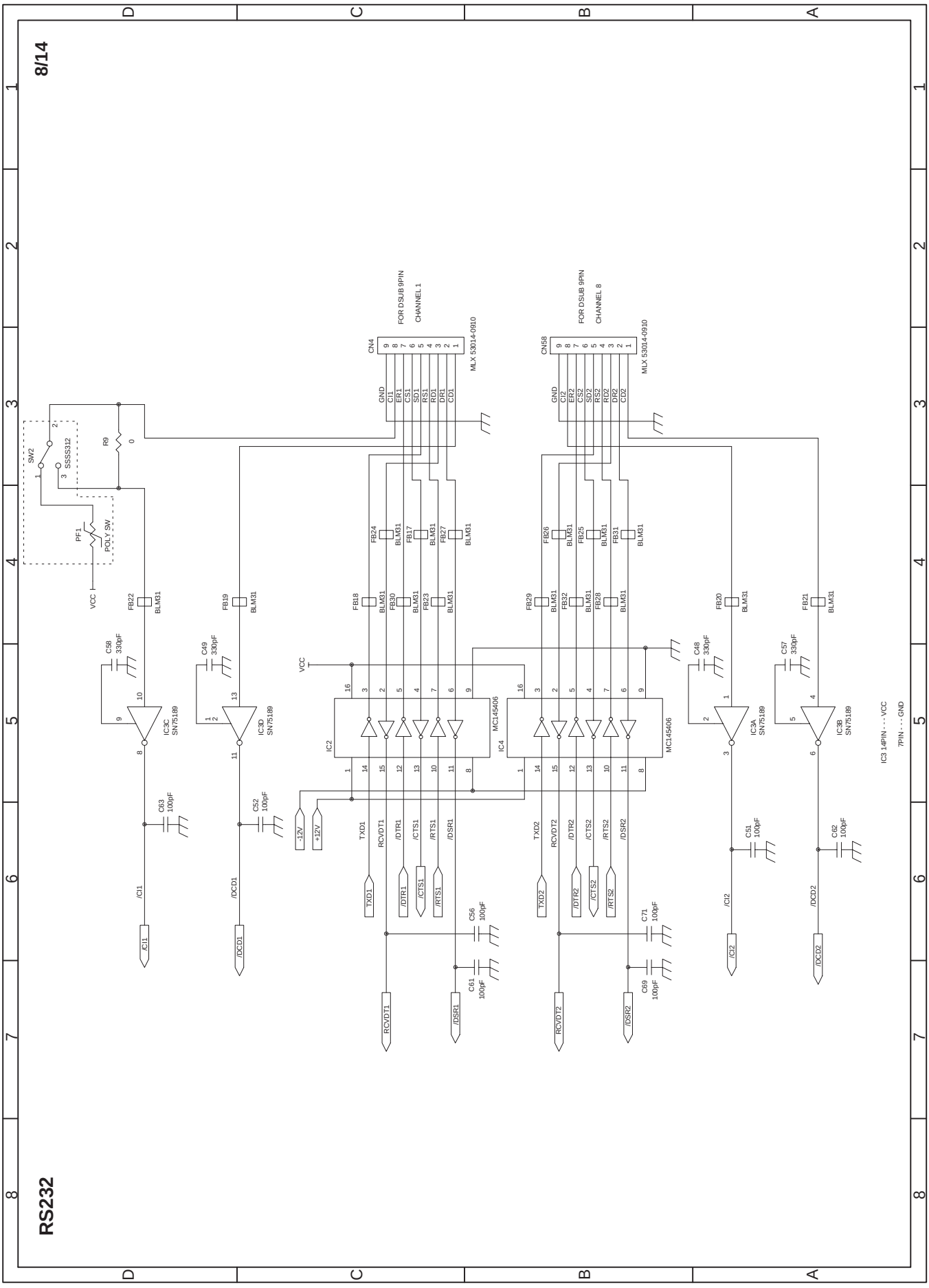

3/14
FLASH ROM
D[8..15]
D[0..7]
IC35
LH28F016SUT
(BE1H#)
A[0..20]
A21
/A21
NOT USED
IC47
7S04FU
R209
R204
0
R203
1K
C213
100pF
C34
10uF/16V
C257
0.1uF
IC35 VCC --- GND
/RD
/HWR
/RES
FVPON
/IPLON0
/FROS1
NORDY
VCC
GND
NC

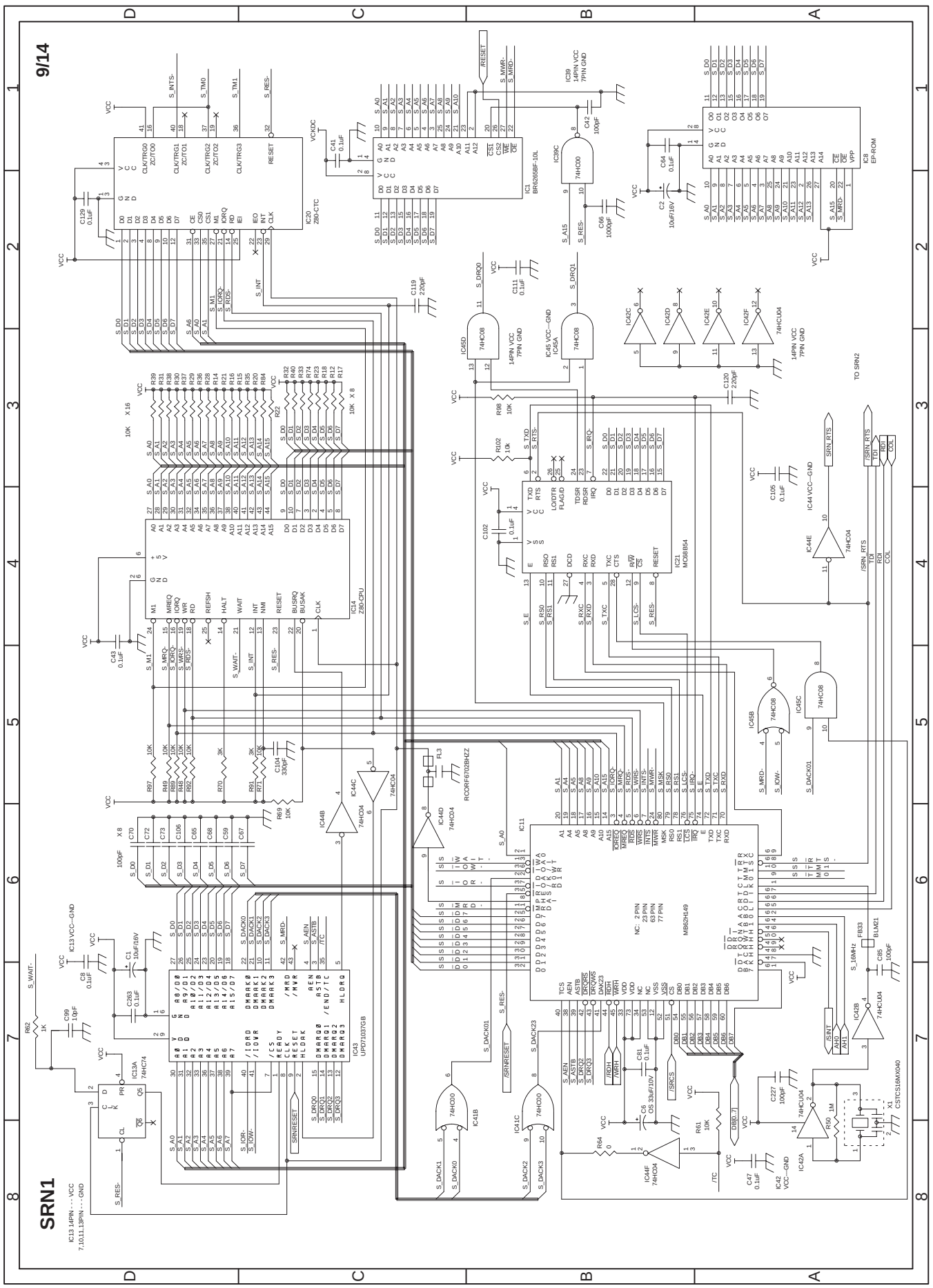

4/14
PSRAM
ODD SIDE
EVEN SIDE
IC33
IC34
IC38
TC51V8512AFT
74AHCT245NS
74LVX00
74LVX32
74LVX08
D[8..15]
D[0..7]
A[1..19]
/PCE1_O
/PCE1_E
/PSREF
/OWR
/HWR
/RESET
/AS
RASPN1
RASPN1E
from MPCA
VCC
VMEM
VCKDC
/MSSWP
/RD
C31
C32
C36
C184
C187
C265
R3
R4
IC22,IC23,IC24,IC25,IC26 VCC --- GND

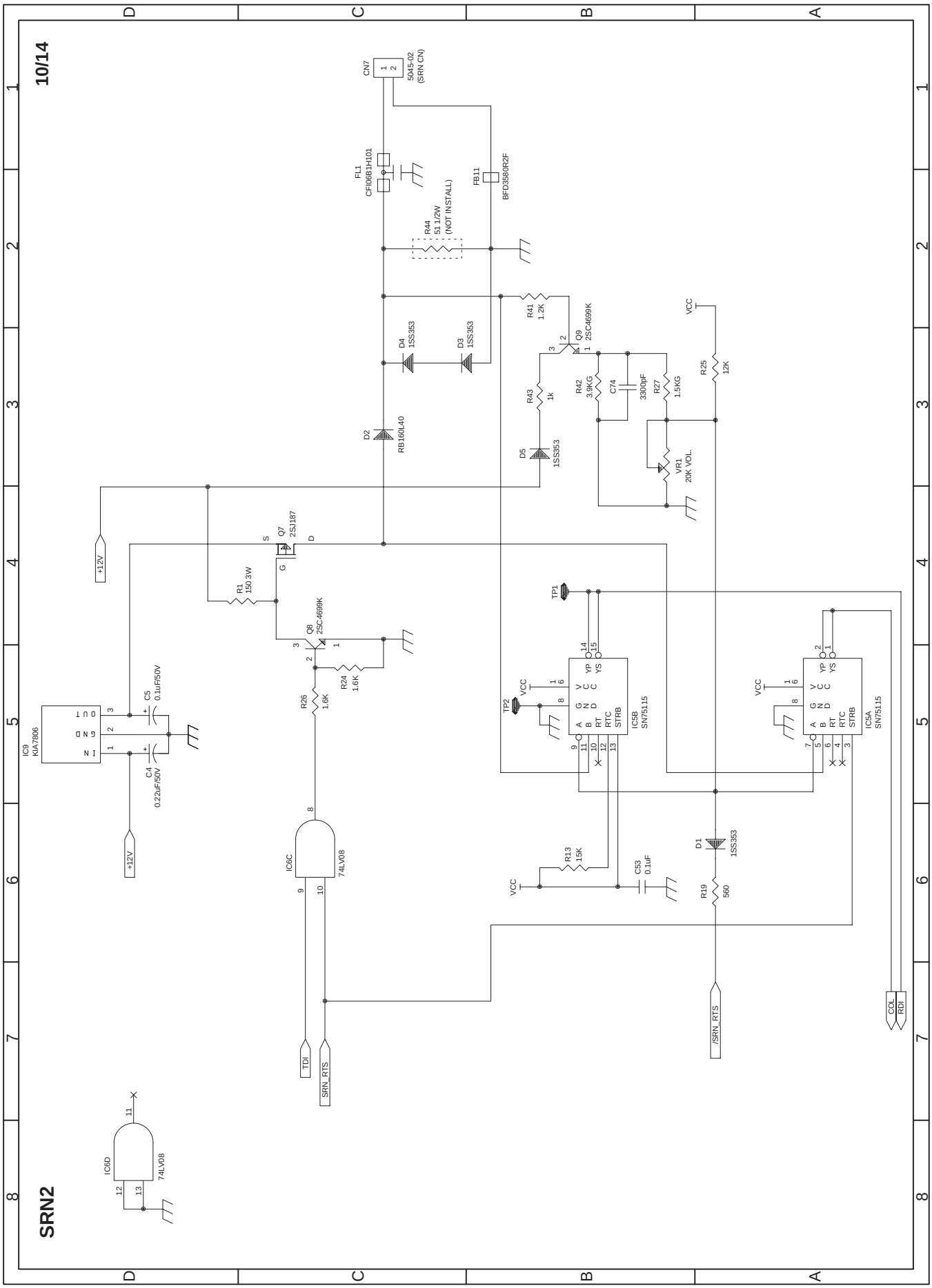

5/14
MPCA8
IC17
MPCA8
VCC
TO CPU
/RES
/VMEM
/FROS1
/MCRINT
/VWAIT
/AS
/RD
/HWR
/#
/RESET
NMI
/IRQ0
RXDI
TXDI
SCKI
/EXWAIT
/WAIT
IPLON0
PHAI
UASCK
/IPLON0
/SHEN2
/TRQ1
/TRQ2
/OPTCS
/EXINT0
/EXINT1
/WRO
/RDO
RCP2
CLS2
RDD2
RCP1
CLS1
RDD1
for MCR
STH2
SCK2
HTS2
STH1
SCK1
HTS1
/POFF
/KRQ
for CKDC CN
D[8..15]
A[0..23]
X2
7.3728MHz
RC8S5P0198CZZ
X3
330pF
X4
X5
100pF
10K
680
1M
10uF/16V
0.1uF

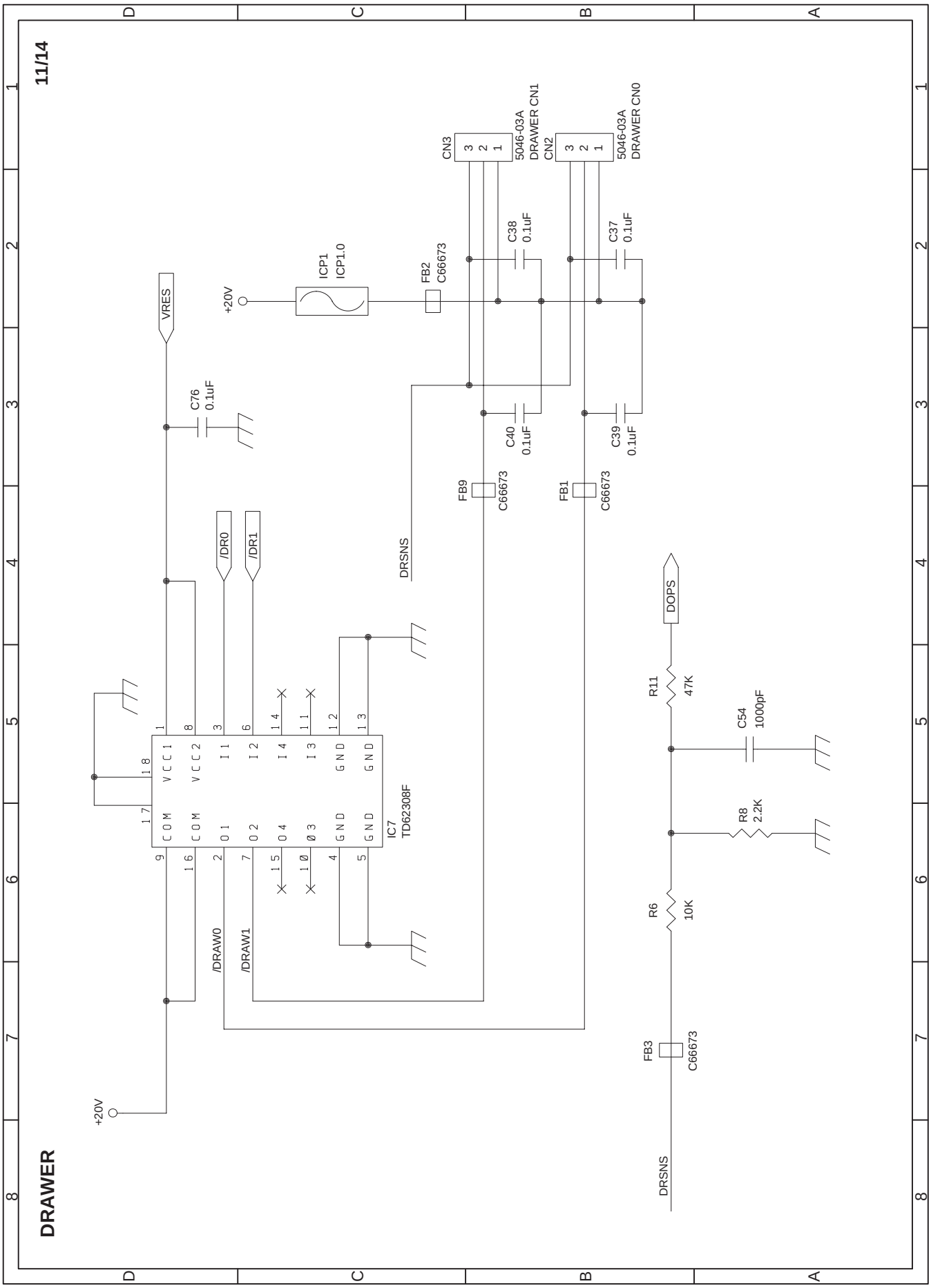

6/14
MCR I/F
CLS1
RDD1
RCP1
CLS2
RDD2
RCP2
R110 10K
R103 10K
R94 10K
R100 10K
R109 10K
R115 10K
R114
R108
R99
R95
R104
VCC
R111 4.7KX6
FB35
FB14
FB37
FB13
FB12
FB40
BLM31 X6
VCC
CLS1#
RDD1#
RCP1#
CLS2#
RDD2#
RCP2#
MCR CN
CN11
8 7 6 5 4 3 2 1
5045-0810

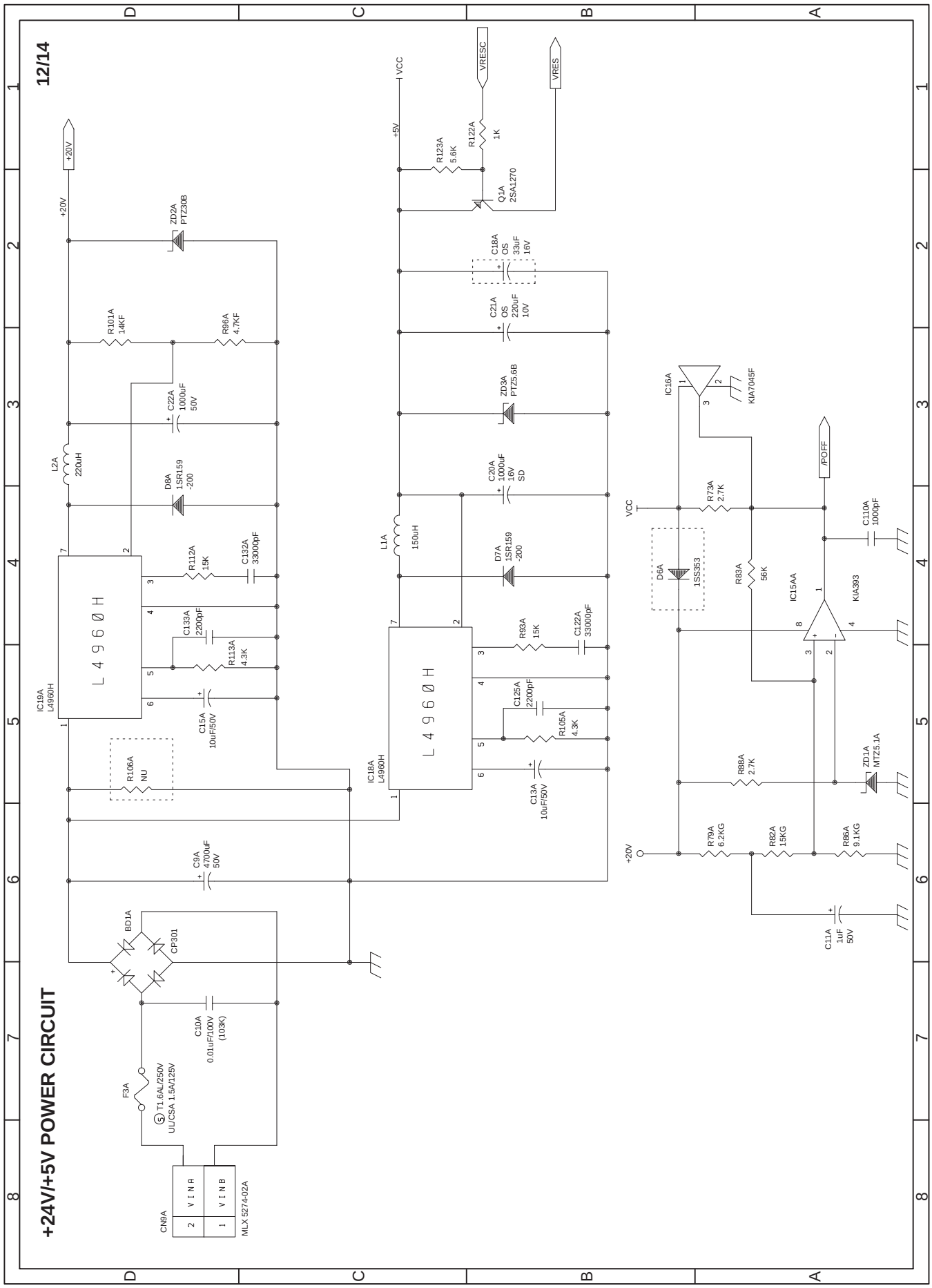

7/14
OPC2
PLZ BE SHORT PATTERN!
IC10
OPC2
CLK_USART
IC6 14PIN - - - VCC
7PIN - - - GND
IC44 14PIN - - - VCC
7PIN - - - GND
74HC04
74LV08
/SRESET
/RES
/SRNRESET
/DCD1
/CTS1
RCVDT1
/CI1
/RTS1
/SINT
/SRCS
/CS1
D[0..15]
A[0..5]
/IRQ1
/IRQ2
/POFF
/WRH
/RDH
DB[0..7]
/DSR1
/DTR1
TXD1
/RES
/WRO
/RDO
/OPTCS
VCC
C7 10uF/16V
C82 0.1uF
C77 NU
R60 10K X10
330pF X10
R59 10K X3
C95
R68 10K
C103 330pF
R65 10K X2
R67
C101
C96 100pF X2
FL2 RCOR6702BHZZ

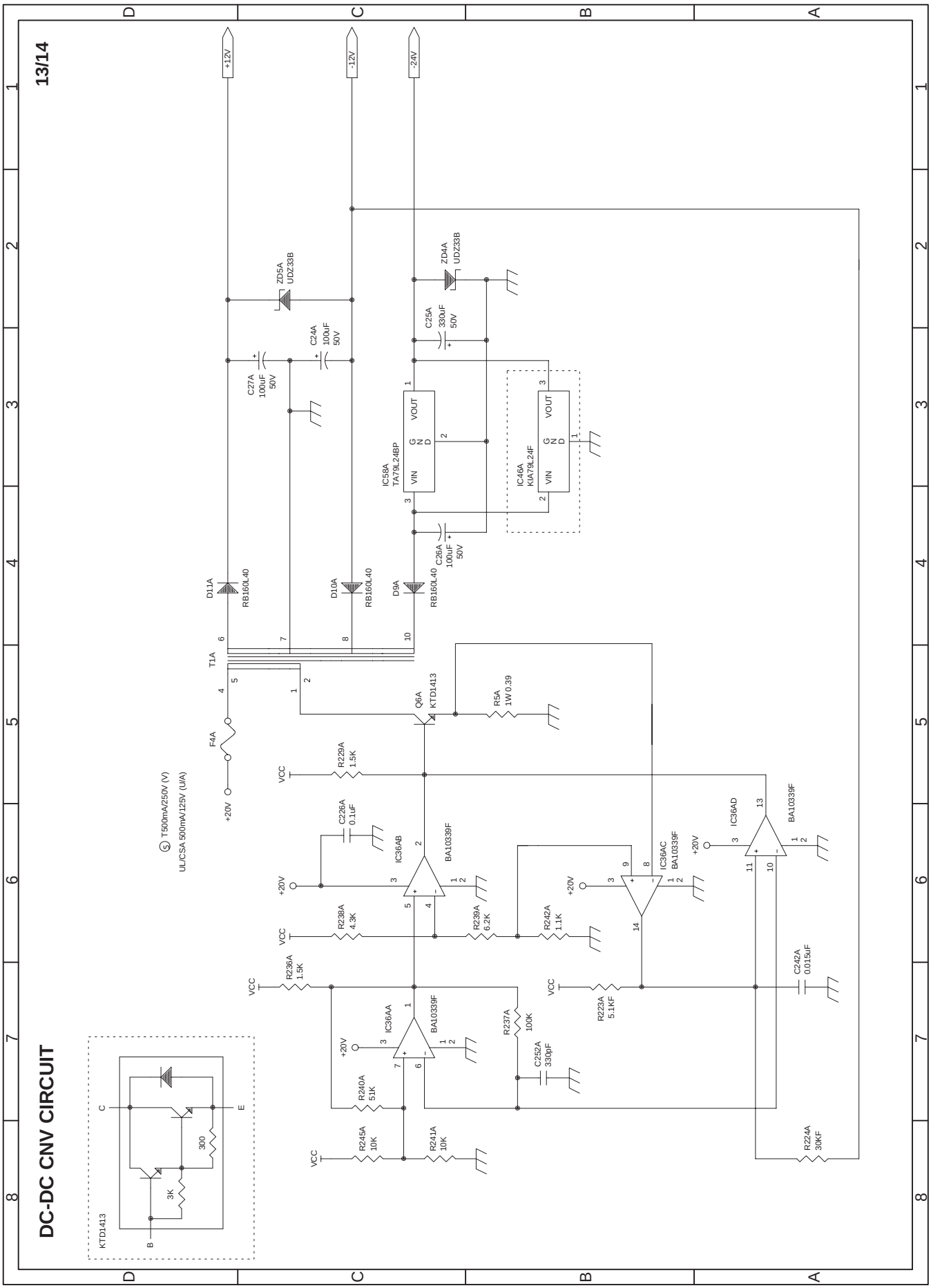

8/14
RS232
SW2
SSSS312
R9
0
PF1
POLY SW
VCC
FB22
BLM31
C58
330pF
IC3C
SN75189
C63
100pF
/CI1
FB19
C49
IC3D
C52
/DCD1
CN4
FOR DSUB 9PIN
CHANNEL 1
MLX 53014-0910
GND
CI1
ER1
CS1
SD1
RS1
RD1
DR1
CD1
FB24
FB17
FB27
FB18
FB30
FB23
IC2
MC145406
-12V
+12V
TXD1
RCVDT1
/DTR1
/CTS1
/RTS1
/DSR1
C56
100pF
C61
100pF
CN58
CHANNEL 8
GND
CI2
ER2
CS2
SD2
RS2
RD2
DR2
CD2
FB26
FB25
FB31
FB29
FB32
FB28
IC4
TXD2
RCVDT2
/DTR2
/CTS2
/RTS2
/DSR2
C71
100pF
C69
100pF
FB20
C48
IC3A
C51
/CI2
FB21
C57
IC3B
C62
/DCD2
IC3 14PIN - - - VCC
7PIN - - - GND

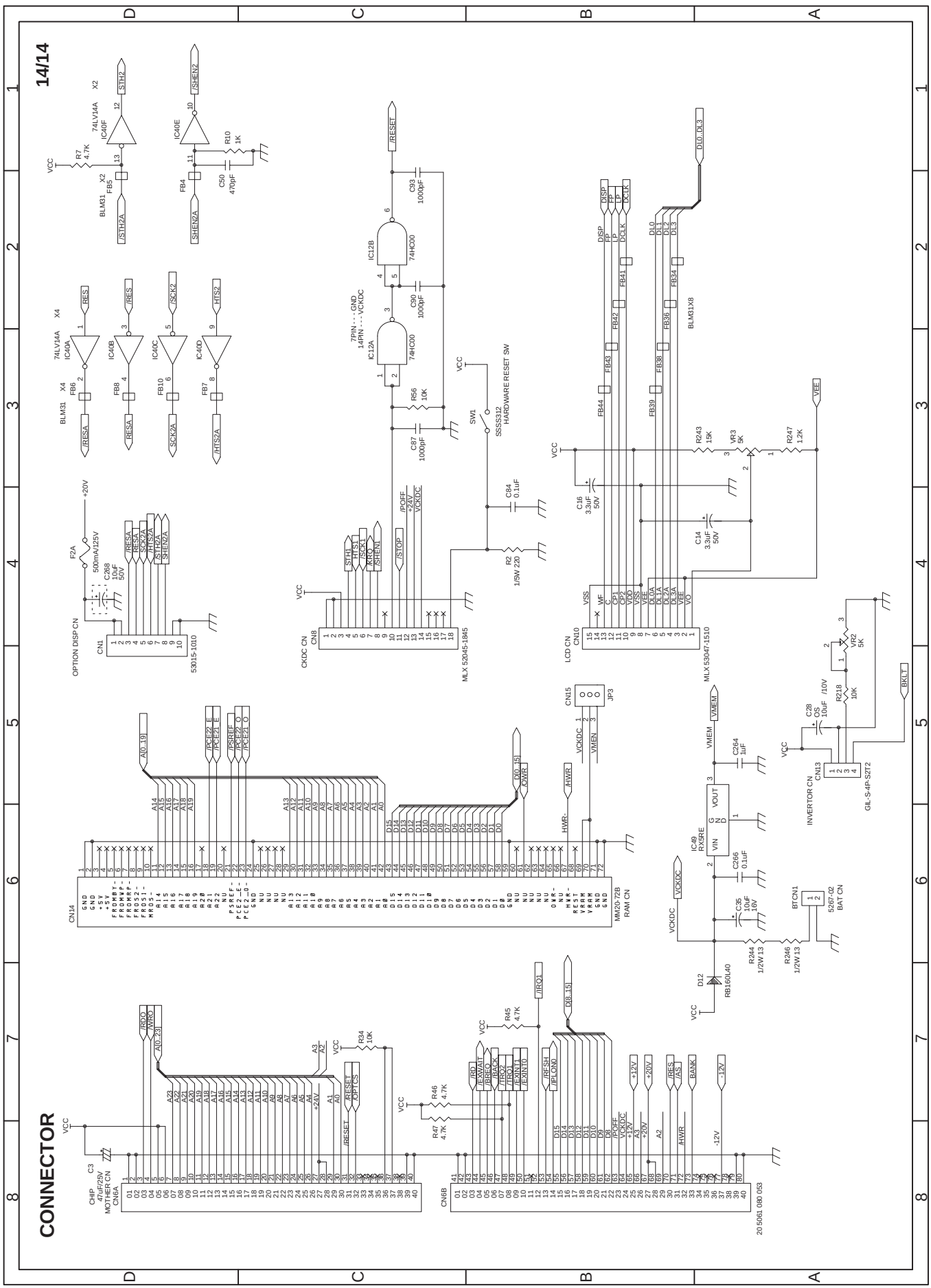

9/14
SRN1
IC13 14PIN - - - VCC
7,10,11,13PIN - - - GND

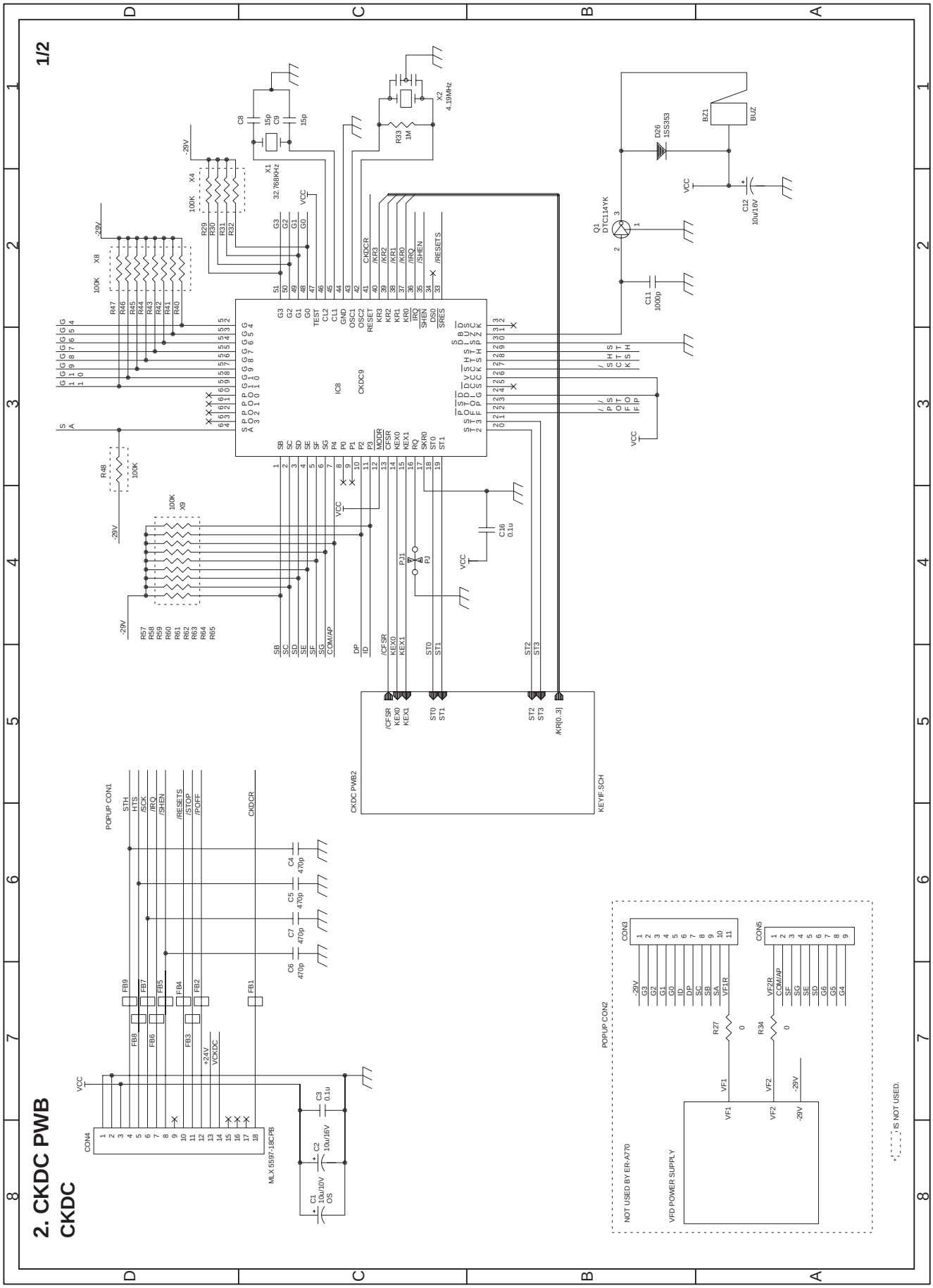

10/14
SRN2
CN7
5045-02
(SRN CN)
FL1
CFI06B1H101
FB11
BFD3580R2F
R44
51 1/2W
(NOT INSTALL)
R41
1.2k
Q9
2SC4699K
D4
1SS353
D3
1SS353
R43
1k
R42
3.9KG
C74
3300pF
R27
1.5KG
R25
12K
VCC
D2
RB160L40
D5
1SS353
VR1
20K VOL.
Q7
2SJ187
+12V
R1
150 3W
Q8
2SC4699K
TP1
TP2
R24
1.6K
R26
1.6K
IC9
KIA7806
C5
0.1uF/50V
C4
0.22uF/50V
IC5B
SN75115
IC5A
SN75115
IC6C
74LV08
IC6D
74LV08
R13
15K
C53
0.1uF
D1
1SS353
R19
560
TDI
SRN_RTS
/SRN_RTS
COL
RDI

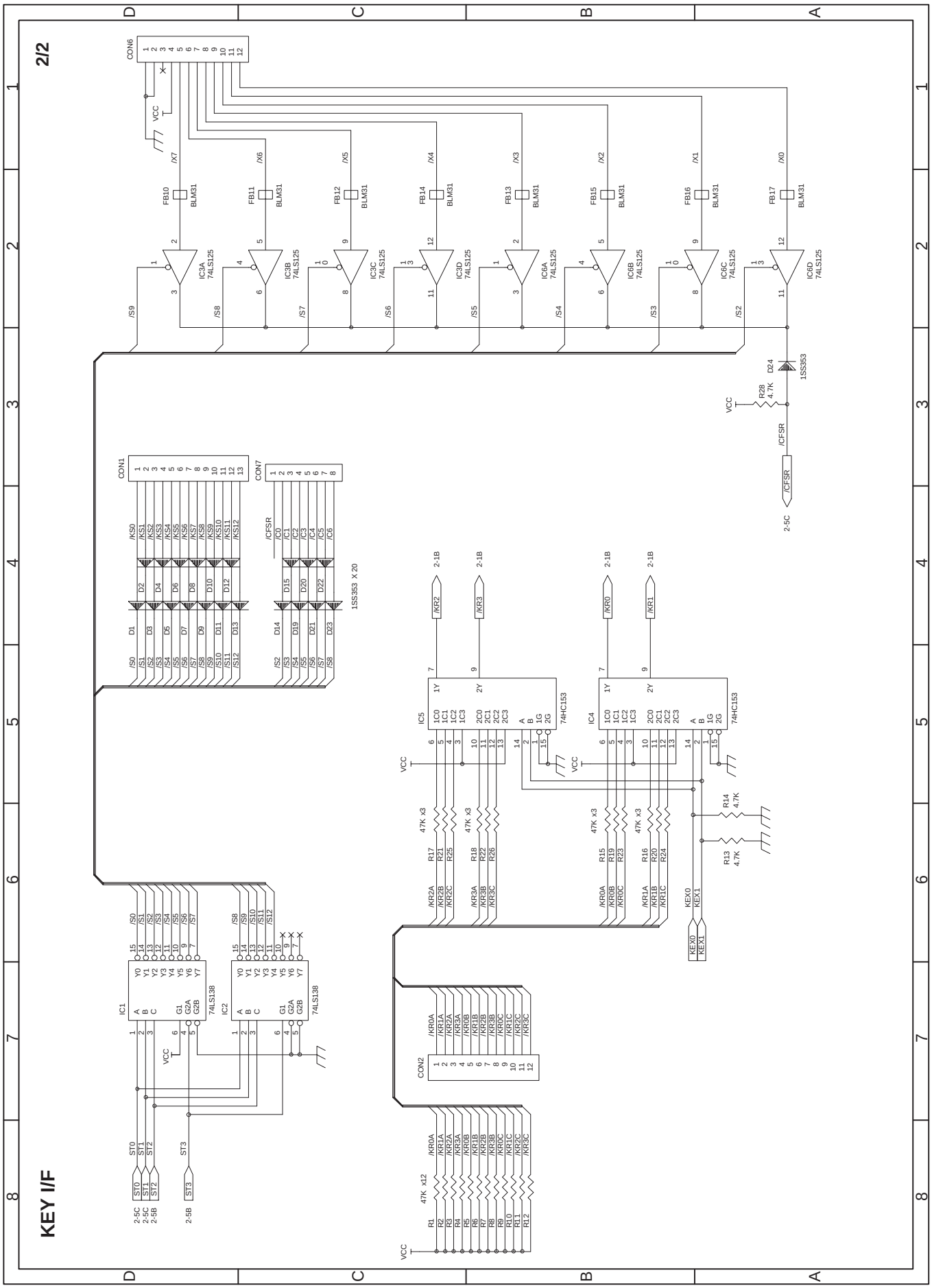

11/14
DRAWER
+20V
VRES
C76
0.1uF
ICP1
ICP1.0
FB2
C66673
CN3
5046-03A
DRAWER CN1
CN2
5046-03A
DRAWER CN0
C38
0.1uF
C37
0.1uF
C40
0.1uF
C39
0.1uF
FB9
C66673
FB1
C66673
/DR0
/DR1
DRSNS
IC7
TD62308F
/DRAW0
/DRAW1
DOPS
R11
47K
C54
1000pF
R8
2.2K
R6
10K
FB3
C66673
DRSNS

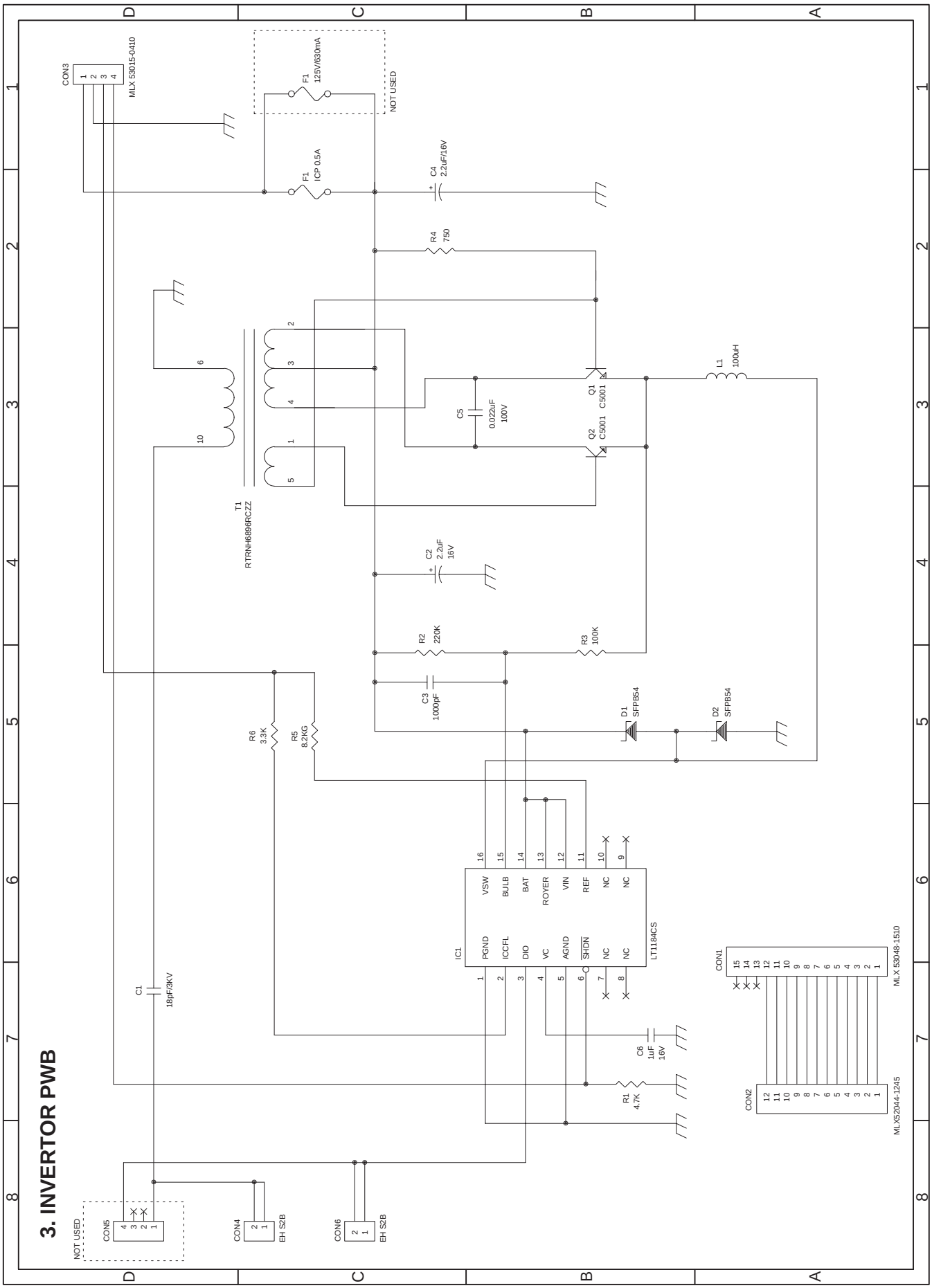

12/14
+24V/+5V POWER CIRCUIT
+20V
+5V
VCC
VRESC
VRES
/POFF
L4960H
IC19A L4960H
IC18A L4960H
IC15AA KIA393
IC16A KIA7045F
CN9A
MLX 5274-02A
VIN B
VIN R
F3A
T1.6AL/250V
UL/CSA 1.5A/125V
BD1A
CP301
L2A 220uH
L1A 150uH
D8A 1SR159 -200
D7A 1SR159 -200
D6A 1SS353
ZD2A PTZ30B
ZD3A PTZ5.6B
ZD1A MTZ5.1A
Q1A 2SA1270
R101A 14KF
R96A 4.7KF
R112A 15K
R106A NU
R113A 4.3K
R93A 15K
R105A 4.3K
R123A 5.6K
R122A 1K
R73A 2.7K
R83A 56K
R88A 2.7K
R79A 6.2KG
R82A 15KG
R86A 9.1KG
C22A 1000uF 50V
C132A 33000pF
C133A 2200pF
C15A 10uF/50V
C9A 4700uF 50V
C10A 0.01uF/100V (103K)
C13A 10uF/50V
C125A 2200pF
C122A 33000pF
C18A OS 33uF 16V
C21A OS 220uF 10V
C20A 1000uF 16V SD
C110A 1000pF
C11A 1uF 50V


13/14
DC-DC CNV CIRCUIT
+12V
-12V
-24V
ZD5A UDZ33B
ZD4A UDZ33B
C24A 100uF 50V
C25A 330uF 50V
C27A 100uF 50V
C26A 100uF 50V
IC58A TA79L24BP
IC46A KIA79L24F
VIN GND VOUT
D11A RB160L40
D10A RB160L40
D9A RB160L40
T1A
F4A
T500mA/250V (V)
UL/CSA 500mA/125V (U/A)
+20V
Q6A KTD1413
R5A 1W 0.39
R229A 1.5K
VCC
C226A 0.1uF
IC36AB BA10339F
IC36AC BA10339F
IC36AD BA10339F
IC36AA BA10339F
R238A 4.3K
R239A 6.2K
R242A 1.1K
R236A 1.5K
R237A 100K
R223A 5.1KF
C242A 0.015uF
C252A 330pF
R240A 51K
R245A 10K
R241A 10K
R224A 30KF
KTD1413
C
B
E
300
3K

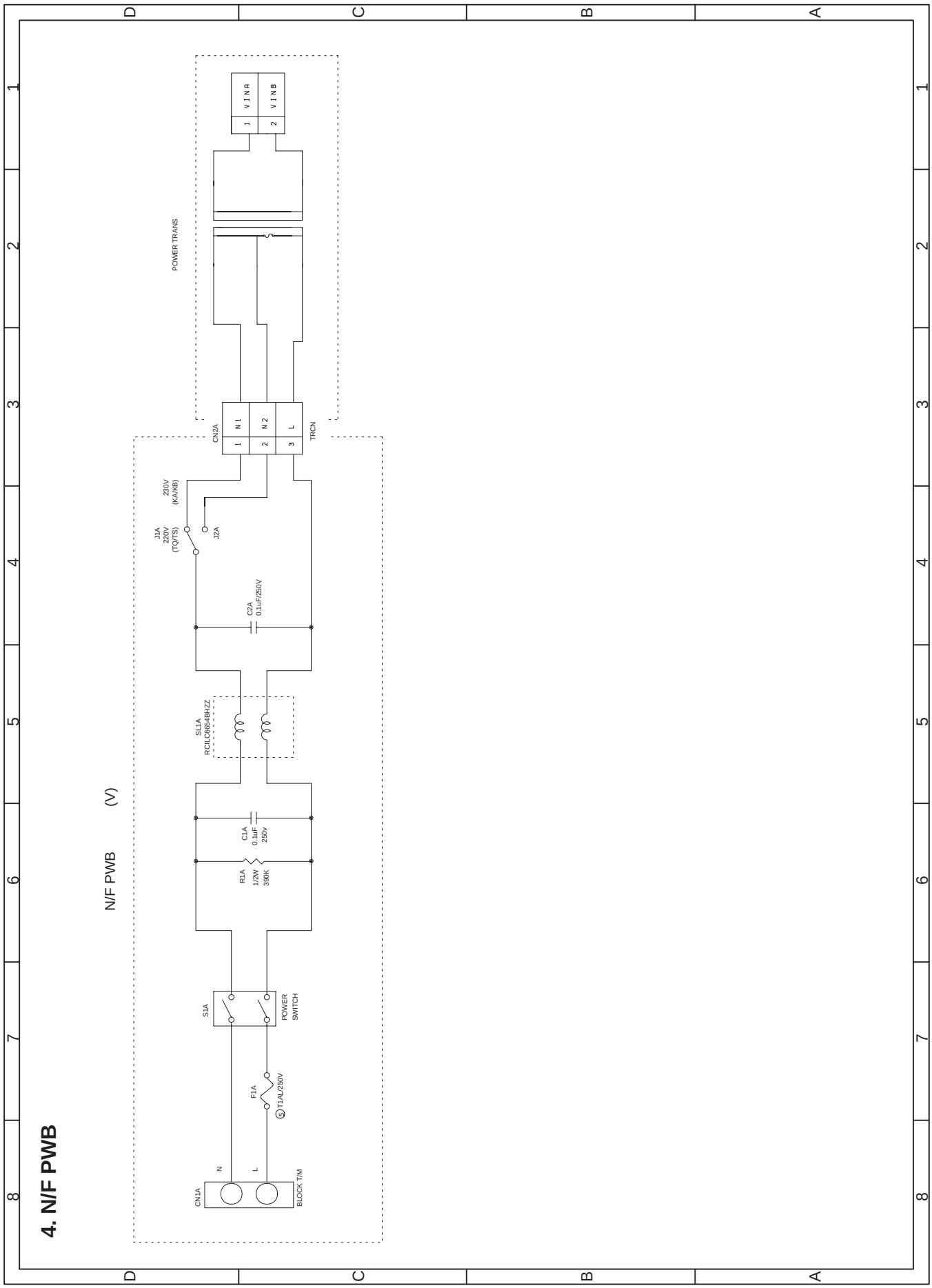

14/14
CONNECTOR
CHIP 47uF/25V MOTHER CN
CN6A
CN6B
20 5061 080 053
OPTION DISP CN
CN1
53015-1010
CKDC CN
CN8
MLX 52045-1845
LCD CN
CN10
MLX 53047-1510
RAM CN
CN14
MM20-72B
INVERTOR CN
CN13
GIL-S-4P-S2T2
BAT CN
BTCN1
5267-02
SW1
SSSS312
HARDWARE RESET SW
JP3
CN15
VCKDC
VMEM
BKLT
VCC
VEE
+20V
-12V
+12V
+24V
/RESET
/IRES
/IRESA
/RESA
/SCK2A
/HTS2A
/STH2A
/SHEN2A
/STOP
/POFF
/IRD
/IWRO
/IWR
/IRQ1
/IRSH
/IPLON0
/EXWAIT
/BREQ
/BACK
/IRQ7
/IRQ11
/EXIN11
/EXIN10
/HWR
/OWR
/PCE22_E
/PCE21_E
/PCE22_O
/PCE21_O
/PSREF
A0..19
D0..15
D8..15
DL0..DL3
IC49 RX5RE
IC40 74LV14A
IC12 74HC00
RB160L40
MM20-72B


1/2
2. CKDC PWB
CKDC
IC8
CKDC9
CKDC PWB2
KEYIF SCH
POPUP CON1
POPUP CON2
CON4
MLX 5597-18CPB
CON3
CON5
NOT USED BY ER-A770
VFD POWER SUPPLY
IS NOT USED.
X1 32.768KHz
X2 4.19MHz
BZ1 BUZ
D26 1SS353
Q1 DTC114YK
C1 10u/10V
C2 10u/16V
C3 0.1u
C4 470p
C5 470p
C6 470p
C7 470p
C8 15p
C9 15p
C11 1000p
C12 10u/16V
C16 0.1u
R27 0
R34 0
R33 1M
VCC
-29V
+24V
VCKDC
CKDCR
/RESETS
/STOP
/POFF
/IRQ
/SHEN
/CFSR
KEX0
KEX1
ST0
ST1
ST2
ST3
/KR[0..3]


2/2
KEY I/F
CON6
VCC
/X7
/X6
/X5
/X4
/X3
/X2
/X1
/X0
FB10
FB11
FB12
FB14
FB13
FB15
FB16
FB17
BLM31
IC3A 74LS125
IC3B 74LS125
IC3C 74LS125
IC3D 74LS125
IC6A 74LS125
IC6B 74LS125
IC6C 74LS125
IC6D 74LS125
/S9
/S8
/S7
/S6
/S5
/S4
/S3
/S2
D24
1SS353
R28
4.7K
/CFSR
2-5C
CON1
CON7
/KS0
/KS1
/KS2
/KS3
/KS4
/KS5
/KS6
/KS7
/KS8
/KS9
/KS10
/KS11
/KS12
/C0
/C1
/C2
/C3
/C4
/C5
/C6
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D19
D20
D21
D22
D23
/S0
/S1
/S2
/S3
/S4
/S5
/S6
/S7
/S8
/S9
/S10
/S11
/S12
1SS353 X 20
IC5
IC4
74HC153
/KR2
/KR3
/KR0
/KR1
2-1B
47K x3
R17
R21
R25
R18
R22
R26
R15
R19
R23
R16
R20
R24
/KR2A
/KR2B
/KR2C
/KR3A
/KR3B
/KR3C
/KR0A
/KR0B
/KR0C
/KR1A
/KR1B
/KR1C
R14
4.7K
R13
4.7K
KEX0
KEX1
IC1
IC2
74LS138
ST0
ST1
ST2
ST3
2-5B
CON2
47K x12
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12

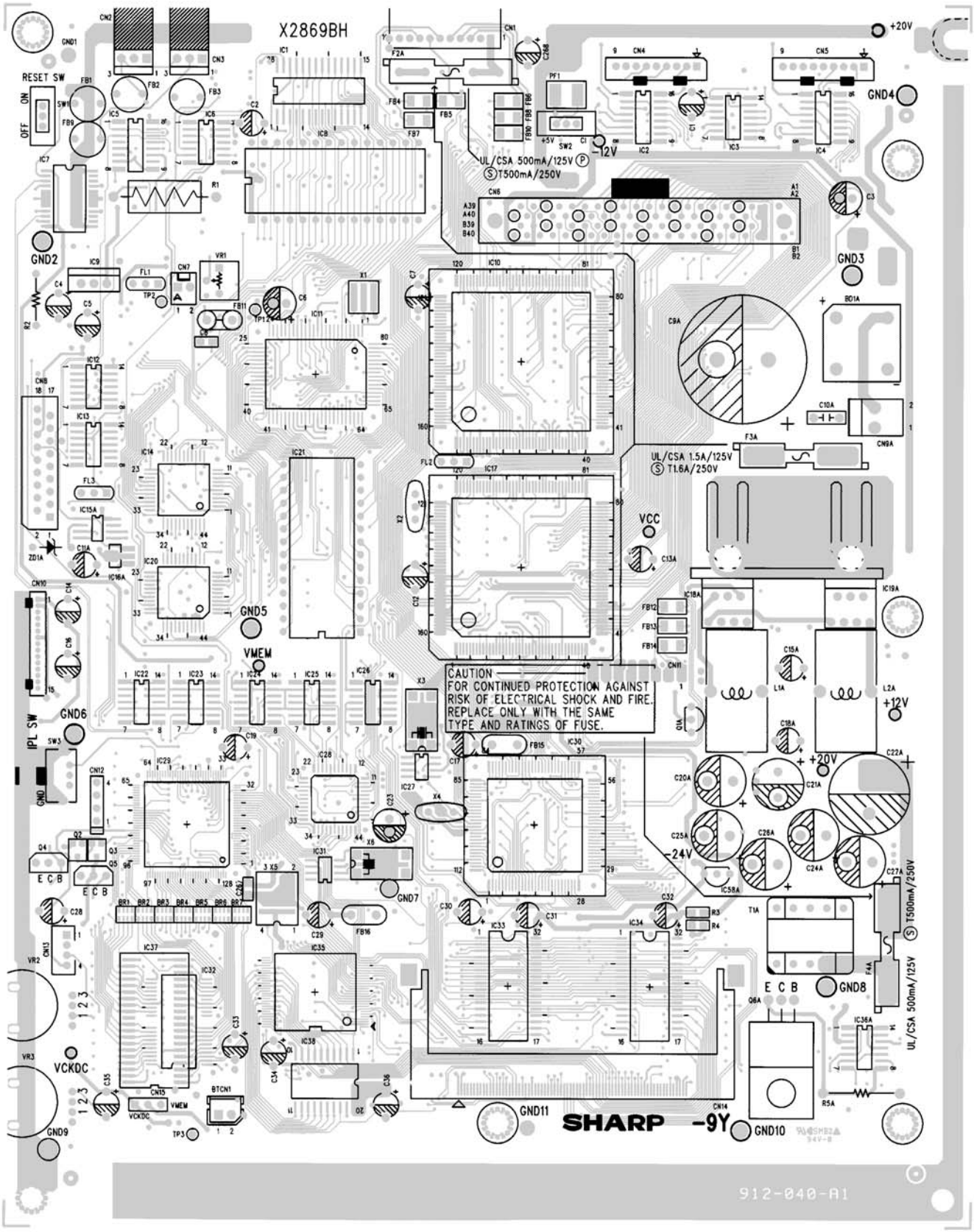

3. INVERTOR PWB
CON3
MLX 53015-0410
F1
125V/630mA
NOT USED
F1
ICP 0.5A
C4
2.2uF/16V
R4
750
T1
RTRNH6896RCZZ
C5
0.022uF
100V
Q1
C5001
Q2
C5001
L1
100uH
C2
2.2uF
16V
R2
220K
R3
100K
C3
1000pF
D1
SFPB54
D2
SFPB54
R6
3.3K
R5
8.2KG
IC1
LT1184CS
VSW
BULB
BAT
ROYER
VIN
REF
NC
NC
PGND
ICCFL
DIO
VC
AGND
SHDN
NC
NC
C1
18pF/3KV
C6
1uF
16V
R1
4.7K
CON1
MLX 53048-1510
CON2
MLX52044-1245
NOT USED
CON5
CON4
EH S2B
CON6
EH S2B

4. N/F PWB

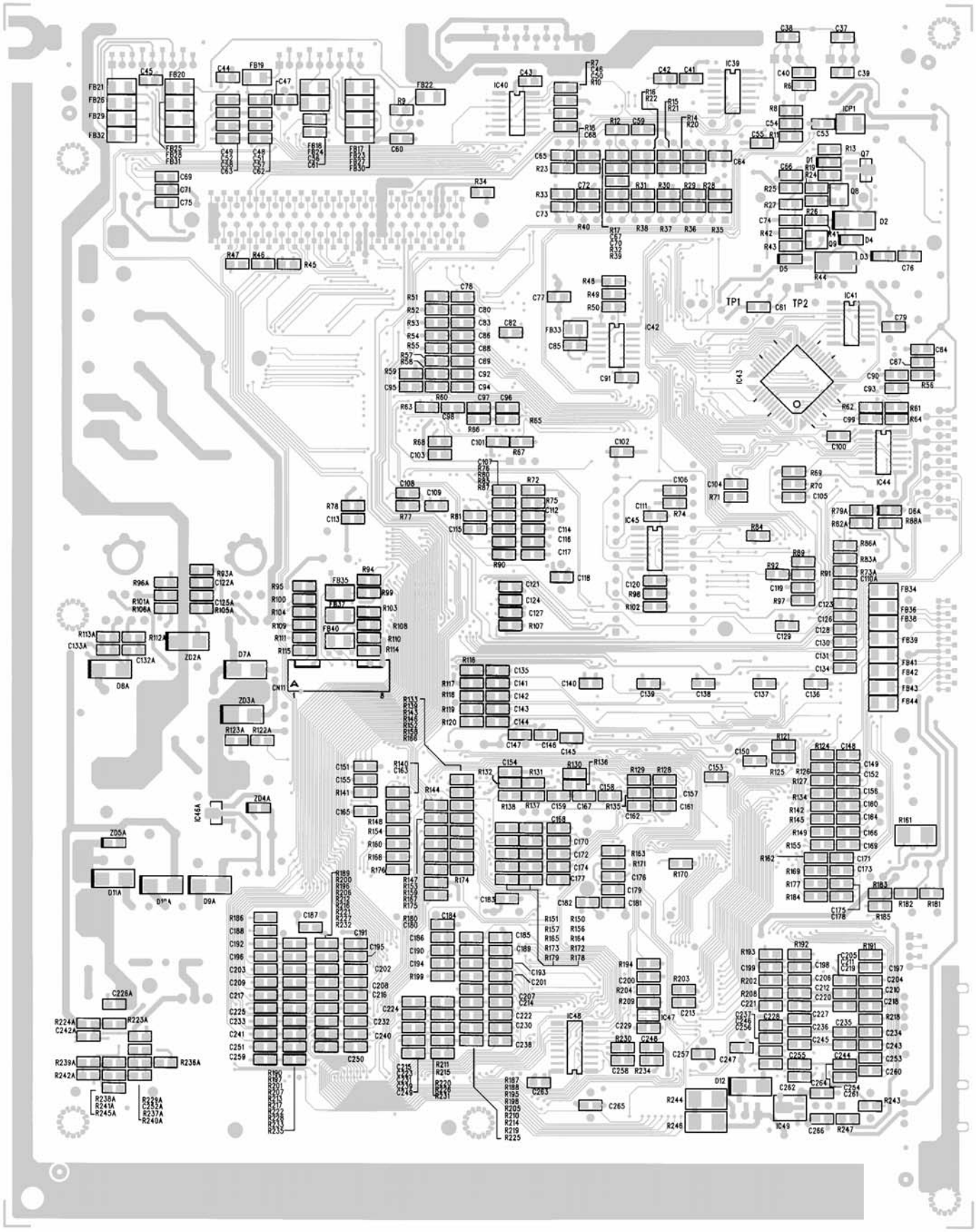

N/F PWB (V)
POWER TRANS
VINA
VINB
CN2A
N1
N2
L
TRCN
230V (KA/KB)
J1A 220V (TQ/TS)
J2A
C2A 0.1uF/250V
SL1A RCILC6654BHZZ
C1A 0.1uF 250v
R1A 1/2W 390K
S1A
POWER SWITCH
F1A
T1AL/250V
CN1A
N
L
BLOCK T/M

CHAPTER 9. PWB LAYOUT

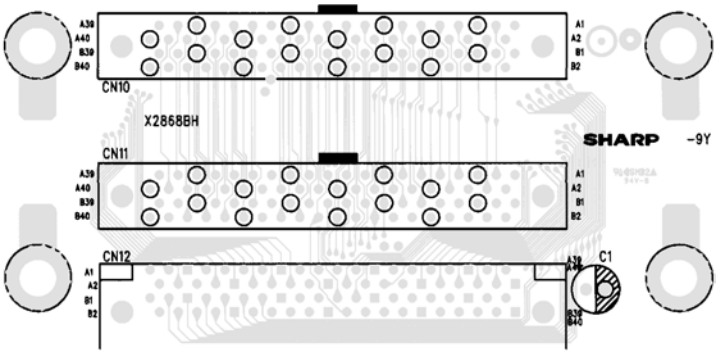
1. Main PWB (Side-A)



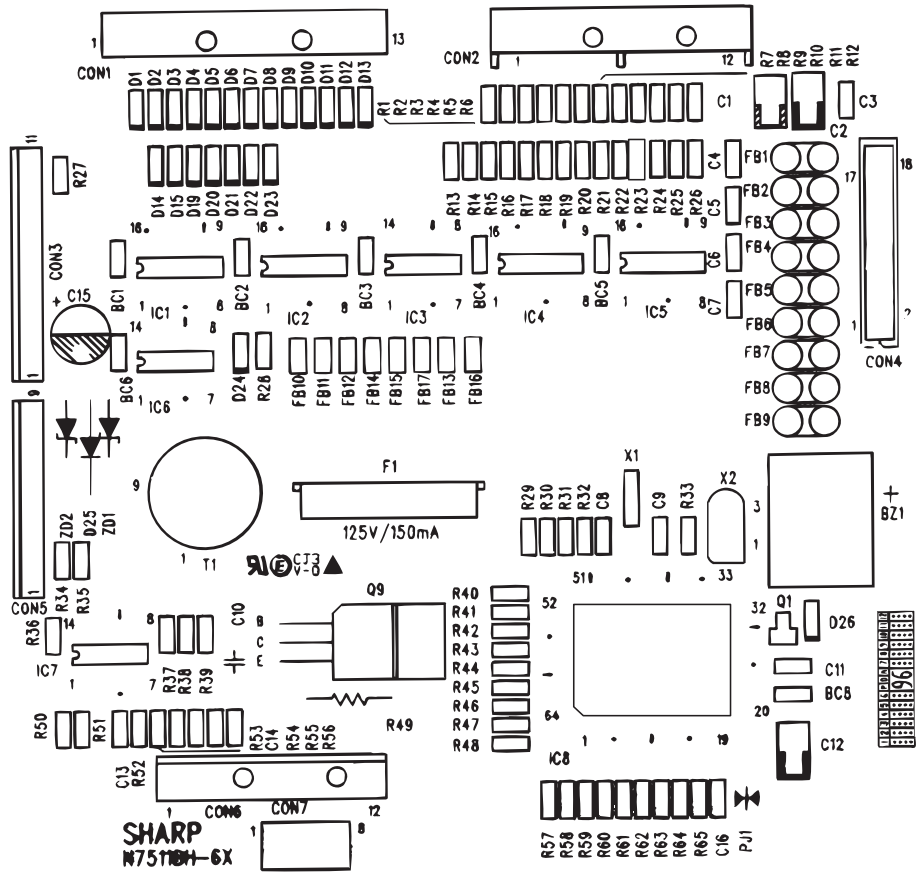
2. Main PWB (Side-B)



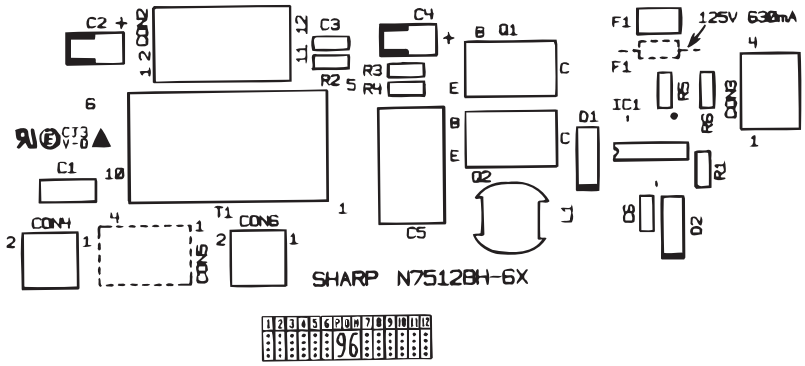
3. Mother PWB



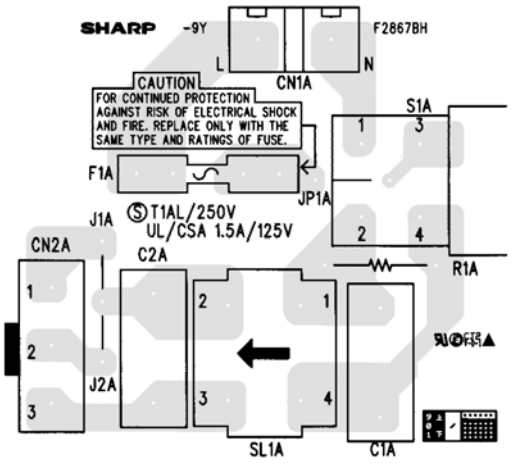
4. CKDC PWB



5. Invator PWB



6. Noise filter PWB



SHARP PARTS GUIDE

MODEL ER-A770

(for TQ,TS,KA,KB)

CONTENTS

1 Top cabinet etc.
2 Bottom cabinet etc.
3 Packing material & Accessories
4 Main PWB unit
5 Mother PWB unit
6 CKDC PWB unit
7 N/F PWB unit
8 Invertor PWB unit
9 Service tools
10 Supply
■ Index

Because parts marked with "⚠" are indispensable for the machine safety maintenance and poeration, it must be replaced with the parts specific to the product specification.

Table of destinations

SELECTION CODE	COUNTRIES
U	U.S.A., Guam
A	Canada
TS	Germany
TQ	SEEG territory other than Germany (Stamp:English)
TR	SEEG territory other than Germany (Stamp:English)
TM	SEEG(FRANCE:Metro-VM) (Stamp:French)
KB	U.Kingdom
KA	Australia

SELECTION CODE	COUNTRIES
K	Korea

SELECTION CODE	COUNTRIES
SB	Saudi Arabia (127V area)
SBA	Saudi Arabia (220V area)
SC	Taiwan
SD	Venezuela
SE	Hong Kong
SG	Lebanon, Syria, Greece, Pakistan, Iran, Egypt, Thailand, Iraq, Mauritius, Seychelles, Tahiti, Jordan, Sudan, Turkey
SH	South Africa (U.S.A. version)
SHE	South Africa (Europe version)
SJ	Philippines (Europe version)
SJ2	Philippines (U.S.A. version)
SM	Kuwait, Qatar, Oman, UAE, Malta, Bahrain
SMT	Nigeria, Yemen, Kenya

SELECTION CODE	COUNTRIES
RA1	Morocco, Algeria, Tunisia, West Africa
RA2	Chile, Uruguay, Peru, Argentina, Paraguay
RA5	Sri Lanka

SELECTION CODE	COUNTRIES
RB3	Indonesia
RB4	
RB5	Cyprus
RB6	Panama
RB7	Barbados
RB8	Malaysia (U.S.A. version)

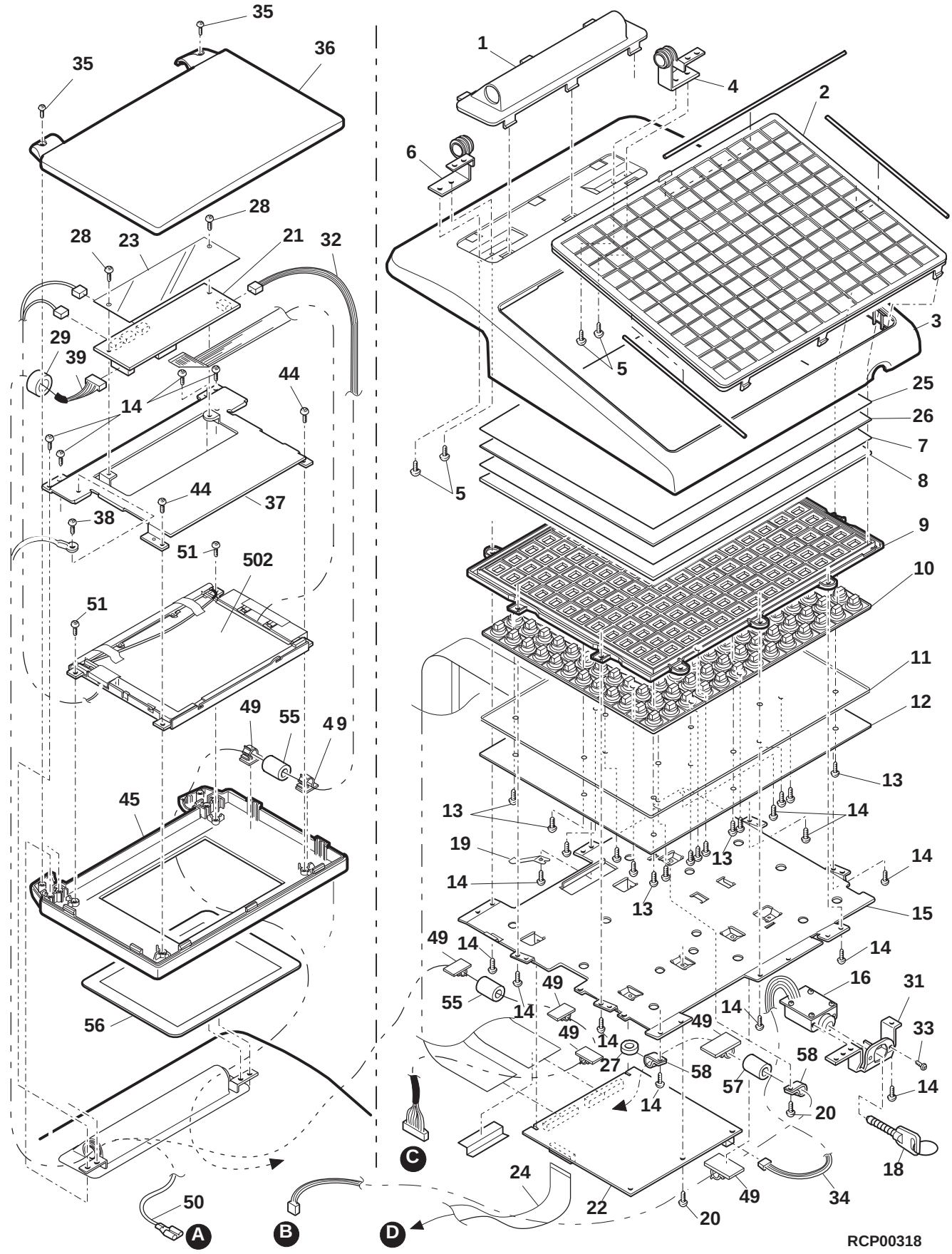
SELECTION CODE	COUNTRIES
RC1	Malaysia (Europe version)
RC2	Singapore
RC5	Dominican Republic, Ecuador

[redacted]
ER-A770V

1 Top cabinet etc.

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GCŌVA7080BHSC	AR	N	D	LCD cover A
2	GCŌVB2503BHZZ	BR	N	D	Key cover A
3	GCABB7202BHSC	BF	N	D	Top cabinet
4	MHNG−6638BHZZ	AU		C	Tilt hinge R
5	XBBSD40P12000	AA		C	Screw (4×12j
6	MHNG−6637BHZZ	AU		C	Tilt hinge L
7	PSHEK6818BHZZ	AQ		C	Blank key sheet
8	GCŌVB7082BHZZ	AZ		D	Key cover B
9	LFRM−6691BHZZ	AZ		D	Key frame
10	PGUMM6712BHZZ	BG		C	Key rubber
11	CSHEP6817BH01	BB		C	Key sheet unit
12	LPLTM6693BHZZ	AX		C	key plate
13	XEBSD30P08000	AA		C	Screw (3×8)
14	XEBSD30P10000	AA		C	Screw (3×10)
15	LANGT7559BHZZ	AW		C	PWB angle A
16	LKGiW7375BHZZ	BG		B	Clerk switch(body)
18	LKGiM7377BH01	AV		B	Clerk key (1)(2pcs/1set,with key ring)
	LKGiM7377BH02	AV		B	Clerk key (2)(2pcs/1set,with key ring)
	LKGiM7377BH03	AV		B	Clerk key (3)(2pcs/1set,with key ring)
	LKGiM7377BH04	AV		B	Clerk key (4)(2pcs/1set,with key ring)
	LKGiM7377BH05	AV		B	Clerk key (5)(2pcs/1set,with key ring)
	LKGiM7377BH06	AV		B	Clerk key (6)(2pcs/1set,with key ring)
19	LANGQ7565BHZZ	AE		C	Earth spring
20	LX−BZ6782BHZZ	AA		C	Screw (3×6)
21	CPWBN7512BH01	BQ		E	Inverter PWB unit
22	CPWBN7511BH03	BR	N	E	CKDC PWB unit
23	GCŌVH7133BHZZ	AH		D	Inverter cover
24	QCNW−7830BHZZ	AQ		C	Flat cable (18pin)
25	PSHEK2904BHZZ	AT	N	C	Standard key sheet
26	PSHEK6852BHZZ	AT		C	Key sheet(programing)
27	RCŌRF6697BHZZ	AF		C	Core (TC18A15)
28	XBBSD30P06000	AA		C	Screw (3×6)
29	RCŌRF6698BHZZ	AR		C	Core (SC18B)
31	LANGK7561BHZZ	AK		C	Clerk angle
32	QCNW−7829BHZZ	AP		C	Inverter cable
33	XJSSD26P08000	AA		C	Screw (2.6×8)
34	QCNW−7832BHZZ	AF		C	Clerk cable (170mm)
35	XEBSF30P08000	AA		C	Screw (3×8)
36	GCABR7256BHSA	AZ	N	D	LCD rear cabinet
37	LPLTM6714BHZZ	AV		C	LCD plate
38	XHBSD30P04000	AA		C	Screw (3×4)
39	QCNW−7828BHZZ	BC		C	LCD cable
44	XEBSD30P06000	AA		C	Screw (3×6)
45	GCABF2551BHZZ	AY	N	D	LCD front cabinet
49	LHLDW6843BHZZ	AE		C	Quick clamp(midle)
50	QCNW−3051BHZZ	AE	N	C	Earth wire (BLACK)
51	XJPSD30P05000	AA		C	Screw (3×5)
55	RCŌRF6695BHZZ	AK		C	Core (OP14A)
56	HDECP2369BHZZ	BA	N	D	LCD panel
57	RCŌRF6699BHZZ	AU		C	Core (BNF28)
58	LHLDW0008SCZZ	AA		C	Cable holder (HP-5N)
501	DUNTK4783BHZZ	BN		E	Key board(flat) [include No.9~13]
502	VVLLM320153−1	BW		E	LCD unit (LM320153)

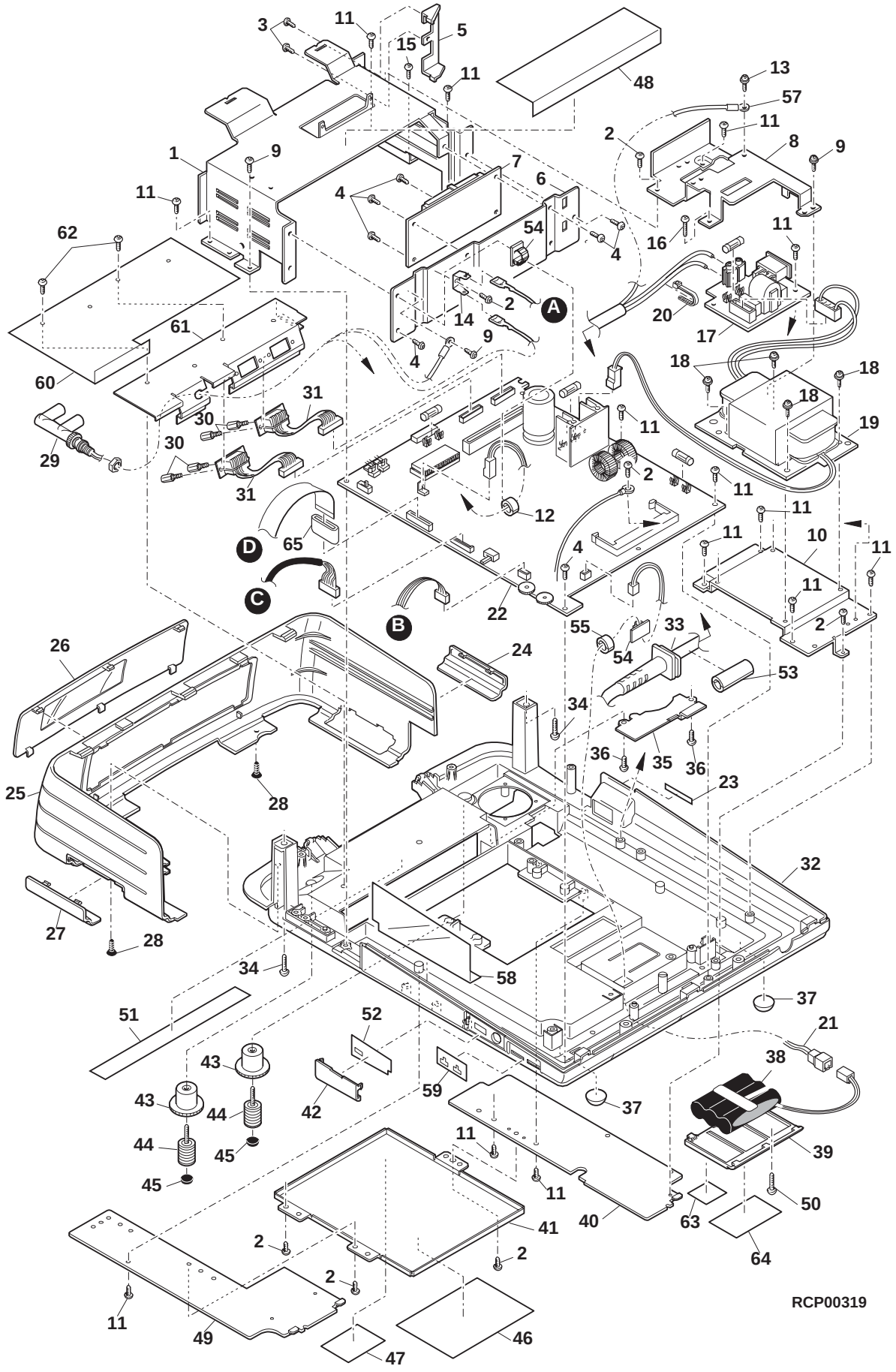
1 Top cabinet etc.



2 Bottom cabinet etc.

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGK7617BHZZ	BA		C	Option angle 1
2	XHBSD30P04000	AA		C	Screw (3×4)
3	XEBSD30P06000	AA		C	Screw (3×6)
4	LX-BZ6782BHZZ	AA		C	Screw (3×6)
5	LANGK7618BHZZ	AQ		C	Option angle 2
6	LANGT7607BHZB	AT	N	C	M/B angle
7	CPWBX2868BH01	BL	N	E	Mother PWB unit
8	LANGK2884BHZZ	AS	N	C	N/F cover
9	XBPSD30P06K00	AA		C	Screw (M3×6K)
10	LANGT2886BHZZ	AU	N	C	Trans plate
11	XEBSD30P08000	AA		C	Screw (3×8)
12	RCŌRF6698BHZZ	AR		C	Core (SC18B)
13	XBPBZ40P06K00	AA		C	Screw (M4×6K)
14	QTANZ6661BHZZ	AE		C	Faston terminal
15	XBBSD30P04000	AA		C	Screw (3×4)
16	LX-BZ6781BHZZ	AB		C	Screw (M3×16)
17	CPWBF2867BH01	BF	N	E	N/F PWB unit
18	XBBSD30P08KS0	AA		C	Screw (3×8KS)
⚠ 19	RTRNP2416BHZZ	BL	N	B	Power transformer [TQ,TS]
⚠ 19	RTRNP2417BHZZ	BL	N	B	Power transformer [KA,KB]
20	LBNDJ2003SCZZ	AA		C	Cable band (Large)
21	QCNW-3091BHZZ	AN	N	C	Battery cable
22	CPWBX2869BH01	CX	N	E	Main PWB unit
23	TLABH7100BHSA	AG	N	D	SW label
24	GFTAS6790BHSC	AH	N	D	Side cover R
25	GCŌVA7085BHZA	BB	N	D	Rear cover
26	GCŌVA7086BHZA	AZ	N	D	Rear d/p cover
27	GFTAS6789BHSC	AH	N	D	Side cover L
28	XJSSF30P12000	AB		C	Screw (M3×12)
29	QCNW-3052BHZZ	AF		C	BNC cable (F-TYPE)
30	LX-BZ6792BHZZ	AF		C	Bolt(d-sub screw)
31	QCNW-7871BHZZ	BC		C	RS232C cable
32	GCABA7205BHZA	BH	N	D	Bottom cabinet
⚠ 33	QACCV6422BHZZ	AY		B	AC cord [TQ,TS]
⚠ 33	QACCL7421BHZZ	AX		B	AC cord (SP-500) [KA]
⚠ 33	QCNW-7212RCZZ	AH		B	AC cord [KB]
34	XUPSD40P12000	AA		C	Screw (M4×12)(M)
35	GFTAS6927BHSA	AM	N	D	AC cord cover
36	XEBSD30P10000	AA		C	Screw (3×10)
37	GLEGG6656BHZZ	AF		D	Gum leg
38	UBATN2338RCZZ	BE		B	Battery (3HR-AAC)
39	GFTAB6788BHSD	AN	N	D	Battery cover
40	LCHSM6707BHZZ	AN		C	Main chssis 1
41	GCŌVH7150BHZZ	AR		D	HDD cover
42	GFTAS6787BHSC	AM	N	D	AT cover
43	GLEGP6658BHSA	AL		D	Tilt leg B
44	GLEGP6657BHSA	AM		D	Tilt leg A
45	GLEGG6659BHZZ	AE		D	T/gum leg
46	TLABG6967BHZZ	AC		D	Battery label
47	TCAUS6677BHZZ	AD		D	Caution label
48	PSHEP6853BHZZ	AG		C	K/B sheet
49	LCHSM6708BHZA	AR	N	C	Main chassis 2
50	XEPSD30P10000	AA		C	Screw (3×10)
51	TLABH7105BHSA	AH	N	D	Connector label
52	PSHEP2918BHZZ	AK	N	C	IPL sheet
53	RCŌRF6695BHZZ	AK		C	Core (OP14A)
54	LHLDW6843BHZZ	AE		C	Quick clamp(midle)
55	RCŌRF6697BHZZ	AF		C	Core (TC18A15)
57	QTANP0004BHZA	AE		C	Earth terminal
58	PSHEP2902BHZZ	AK	N	C	Ventilation hole sheet
59	TLABH7101BHZA	AL		D	Volume label
60	PSHEP2907BHZZ	AP	N	C	Option C/N sheet
61	LANGT2885BHZZ	AS	N	C	Option C/N angle
62	XJSSD30P08000	AA		C	Screw (3×8)
63	TLABH6996BHZZ	AD		D	Battery cover seal [KB]
64	TLABG7097BHZZ	AF		D	Battery caution label
65	RCŌRF6705BHZZ	AM		C	Core (CABLE33)

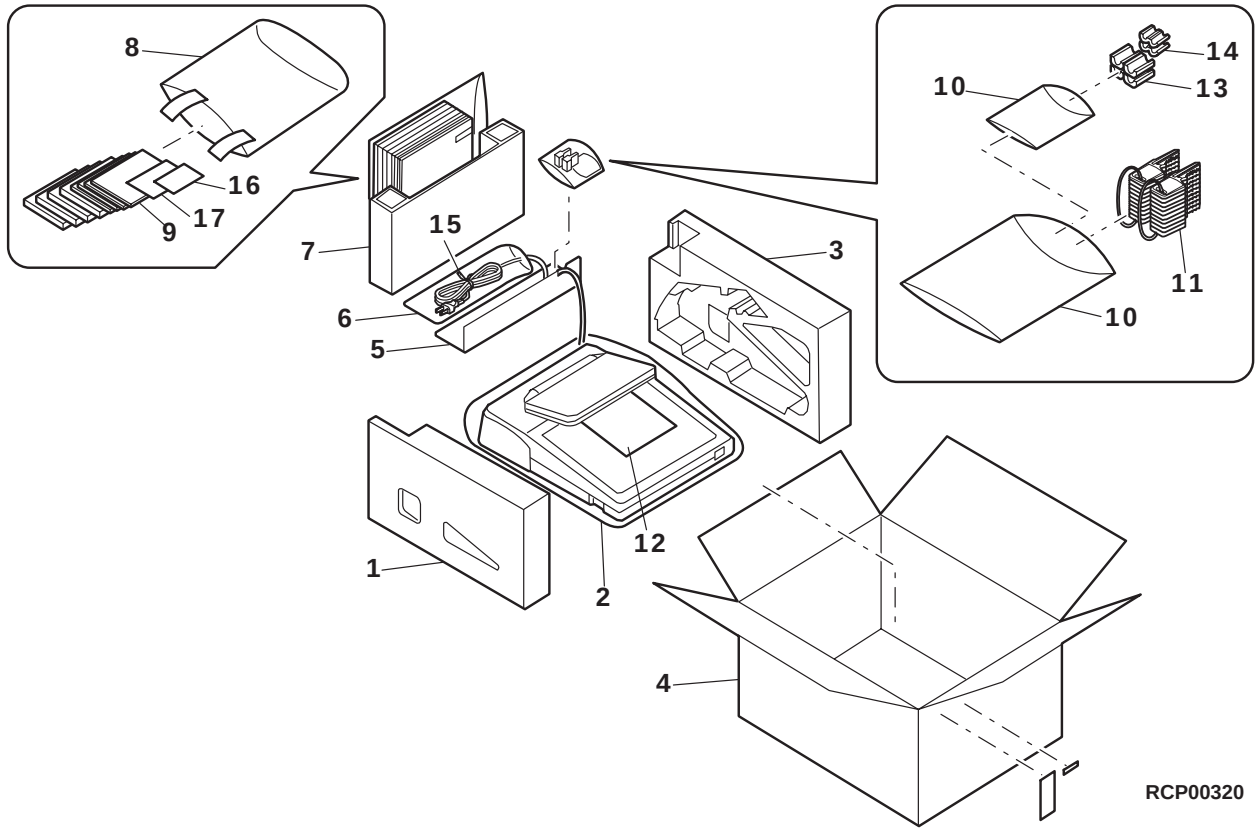
2 Bottom cabinet etc.



3 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKA8409BHAL	AX	N	D	Packing add L
2	SSAKH0003DHZZ	AE		D	Vinyl bag (640×560mm)
3	SPAKA8410BHAR	AX	N	D	Packing add R
4	SPAKC3132BHZZ	BA	N	D	Packing case
5	SPAKA8435BHZZ	AF		D	Pad C
6	SSAKH4231CCZZ	AA		D	Vinyl bag (140×500mm)
7	SPAKA3129BHZZ	AU		D	Pad 1
8	SSAKH0013HCZZ	AA		D	Vinyl sack [TQ,TS]
	SSAKH3015CCZZ	AA		D	Vinyl bag (200×300mm) [KA,KB]
9	TiNSE2407BHZZ	BK	N	D	Instruction book (E1) [TQ,TS]
	TiNSE2411BHZZ	BF	N	D	Instruction book (E2) [TQ,TS]
	TiNSF2409BHZZ	BK	N	D	Instruction book (F1) [TQ,TS]
	TiNSF2413BHZZ	BF	N	D	Instruction book (F2) [TQ,TS]
	TiNSG2408BHZZ	BK	N	D	Instruction book (G1) [TQ,TS]
	TiNSG2412BHZZ	BF	N	D	Instruction book (G2) [TQ,TS]
	TiNSS2410BHZZ	BK	N	D	Instruction book (S1) [TQ,TS]
	TiNSS2414BHZZ	BF	N	D	Instruction book (S2) [TQ,TS]
	TiNSE2420BHZZ	BK	N	D	Instruction book (E1) [KA,KB]
	TiNSE2421BHZZ	BF	N	D	Instruction book (E2) [KA,KB]
10	SSAKA5004CCZZ	AA		D	Vinyl bag (100×300mm)
11	LKGiM7377BH01	AV		B	Clerk key (1)(2pcs/1set,with key ring)
	LKGiM7377BH02	AV		B	Clerk key (2)(2pcs/1set,with key ring)
	LKGiM7377BH03	AV		B	Clerk key (3)(2pcs/1set,with key ring)
	LKGiM7377BH04	AV		B	Clerk key (4)(2pcs/1set,with key ring)
	LKGiM7377BH05	AV		B	Clerk key (5)(2pcs/1set,with key ring)
	LKGiM7377BH06	AV		B	Clerk key (6)(2pcs/1set,with key ring)
12	TCADH6788BHZA	AC		D	Caution card (Black)
13	RCŌRF6699BHZZ	AU		C	Core (BNF28)
14	RCŌRF6700BHZZ	AS		C	Core (BNF-14)
15	UBNDA6629BHZZ	AA		C	AC cord band (4mm×200mm)(Green)
16	TGANE1001BHZC	AG		D	Warranty card [KA]
17	TCADZ2001BHZA	AM		D	Install card [KA]

3 Packing material & Accessories



4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	LX−BZ6644BHZZ	AA		C	Screw (M3.5×8S)	
2	PRDAF2379BHZZ	AS	N	C	Heat sink	
3	QCNCM1060AC03	AB		C	Connector (Short Pin 3P)	[CN15]
4	QCNCM1101BHZZ	AC		C	Connector (5273-2)(2P)	[CN9A]
5	QCNCM2551RC1J	AF		C	Connector (10pin)	[CN1]
6	QCNCM5278NCZZ	AC		C	Connector (3pin)(5046-03A)	[CN2,3]
7	QCNCM7057BH08	AG		C	MCR Connector (5045-0810)	[CN11]
8	QCNCM7075BH0B	AB		C	Connector (5045-03A)	[CN7]
9	QCNCM7128BH1E	AH		C	Connector (MLX 53047-1510)	[CN10]
10	QCNCM7129BH0D	AB		C	Inverter connector (GIL-S-4P-S2T2-EF)(4PIN)	[CN13]
11	QCNCM7222BH0i	AD		C	Connector (MLX53014-0910)	[CN4,5]
12	QCNCW1057ACZZ	AB		C	Connector (Short socket)	[CN15]
13	QCNCW7081BHZZ	AB		C	Connector (2P)(5267-02A)(Blue)	[BTCN1]
14	QCNCW7204RC8J	AM		C	I/O connector (80pin)(10 5061 080)	[CN6]
15	QCNCW7206RC1H	AG		C	CKDC Connector (18PIN)(MLX52045-1845)	[CN8]
⚠ 16	QFS−C1035CCZZ	AE		A	Fuse (1.6A 250V)	[F3A]
⚠ 17	QFS−C5012BHZZ	AF		A	Fuse (T500mAL 250V)	[F2A,4A]
18	QFSHD2109AFZZ	AC		C	Fuse holder (HD2109AF)	[F2A,3A,4A]
19	QSŌCZ1012AC7B	AP		C	Socket (MM20-72B2-1-T24)	[CN14]
20	QSŌCZ6428ACZZ	AE		C	IC socket (28P)	[IC8]
21	QSW−S0744AFZZ	AG		B	Reset switch (SSS312)	[SW1]
22	QSW−S6894BHZZ	AK		B	Slide switch	[SW3]
23	RC−EZ106ARC1A	AD		C	Capacitor (10WV 10μF)	[C19,28,30,31,32]
24	RC−EZ2271RC1A	AM		C	Capacitor (220μF/10V)	[C21A]
25	RC−EZ336ARC1A	AB		C	Capacitor (10WV 33μF)	[C6,23]
26	RCiLC2421BHZZ	AP	N	C	Coil (150μH)	[L1A]
27	RCiLC2422BHZZ	AP	N	C	Coil (220μH)	[L2A]
28	RCiLZ5017SCZ/	AF		C	Chip core (BLM31)	[FB4,5,6,7,8,10,12,13,14]
	RCiLZ5017SCZ/	AF		C	Chip core (BLM31)	[FB17,18,19,20,21,22,23,24]
	RCiLZ5017SCZ/	AF		C	Chip core (BLM31)	[FB25,26,27,28,29,30,31,32]
	RCiLZ5017SCZ/	AF		C	Chip core (BLM31)	[FB34,35,36,37,38,39,40,41]
	RCiLZ5017SCZ/	AF		C	Chip core (BLM31)	[FB42,43,44]
29	RCŌRF1008ACZZ	AB		C	Chip bead (BUM21A05)	[FB33]
30	RCŌRF2337BHZZ	AN		C	Ferrite core	[FB1,2,3,9]
31	RCŌRF6691BHZZ	AD		C	Core (BFS3550R2F)	[FB11]
32	RCŌRF6702BHZZ	AF		C	EMI filter (100pF)	[FL1,2,3]
33	RCRMZ1016LCZZ	AF		B	Crystal (16MHz(CSTCS16MX040))	[X1]
34	RCRSP5019BCZZ	AD		B	Crystal (7.37MHz)	[X2]
35	RCRSP6664RCZZ	AF		B	Crystal (19.66MHz)	[X4]
36	RCRSZ2407RCZZ	AQ	N	B	Chip X-TAL (15MHz)	[X5]
37	RMPTQ4330QCJJ	AC		B	Block resistor (33Ω×4 1/16W ±5%)	[BR1,2,3,4,5,6,RB7]
⚠ 38	RTRNH2419RCZZ	AV	N	B	DC-DC converter (SEE-16)	[T1A]
39	RVR−B2410QCZZ	AG		B	Variable resistor (5K)	[VR2,3]
40	RVR−M2415QCN3	AE		B	Variable resistor (20K)	[VR1]
41	VCCCTV1HH100J	AA		C	Capacitor (50WV 10PF)	[C99]
42	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C42,51,52,56,59,61,62,63,65,67]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C68,69,70,71,72,73,85,96,101]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C106,107,108,112,113,114,115,116]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C117,127,135,141,142,143,144,148]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C155,165,168,170,174,177,180,185]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C186,188,189,190,191,192,193,194]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C195,196,200,201,202,203,207,208]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C209,213,214,215,216,217,220,221]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C233,238,239,240,241,248,249,250]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C251,258,259]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C222,223,224,225,227,230,231,232]
43	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C119,120]
44	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C46,48,49,57,58,78,80,83,86,88]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C89,92,94,95,97,98,103,104,121]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C123,124,128,130,149,152,154,156]
	VCCCTV1HH331J	AA		C	Capacitor (50WV 330PF)	[C157,162,163,171,173,175,178,252A]
45	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C158]
46	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF)	[C50,134]
47	VCCCTV1HH510J	AA		C	Capacitor (50WV 51PF)	[C267]
48	VCEAEU1CW106M	AA		C	Capacitor (16WV 10μF)	[C1,2,7,12,33,34,35,36]
49	VCEAEU1VW476M	AB		C	Capacitor (35WV 47μF)	[C3]
50	VCEAGA1HW104M	AB		C	Capacitor (0.1μF/50V)	[C5]
51	VCEAGA1HW105M	AB		C	Capacitor (50WV 1μF)	[C11A]
52	VCEAGA1HW106M	AA		C	Capacitor (50WV 10μF)	[C13A,15A]
53	VCEAGA1HW107M	AA		C	Capacitor (50WV 100μF)	[C24A,26A,27A]
54	VCEAGA1HW224M	AA		C	Capacitor (50WV 0.22μF)	[C4]
55	VCEAGA1HW335M	AB		C	Capacitor (50WV 3.3μF)	[C14,16]
56	VCEAGD1CW108M	AE		C	Capacitor (16WV 1000μF)	[C20A]
57	VCEAGD1HW337M	AF		C	Capacitor (330μF/50V SD)	[C25A]
58	VCEAGU1HW108M	AF		C	Capacitor (50WV 1000μF)	[C22A]
59	VCEAGU1HW478M	AL		C	Capacitor (50WV 4700μF)	[C9A]
60	VCKYTV1CF105Z	AB		C	Capacitor (1μF 16V)	[C264]
61	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C54,66,87,90,93,110A,153]
62	VCKYTV1HB103K	AB		C	Capacitor (50WV 0.010μF)	[C161]
63	VCKYTV1HB153K	AA		C	Capacitor (50WV 0.015μF)	[C242A]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
64	VCKYTV1HB222K	AA		C	Capacitor (50WV 2200pF)	[C125A,133A]
65	VCKYTV1HB332K	AA		C	Capacitor (50WV 3300PF)	[C74]
66	VCKYTV1HB333K	AA		C	Capacitor (50WV 0.033μF)	[C122A,132A]
67	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C8]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C37,38,39,40,41,43,47,53,55]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C64,76,79,81,82,84,102,105,109]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C111,118,129,136,137,138,139,140]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C150,151,167,182,183,184,187,226A]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C247,257,263,265,266]
68	VCQYNA2AM103K	AA		C	Capacitor (100WV 0.010μF)	[C10A]
69	VHD1SR159//-1	AF		B	Chip diode (1SR159-200)	[D7A,8A]
70	VHD1SS353//-1	AB		B	Diode (1SS353)	[D1,3,4,5]
71	VHDCP301///-1	AL		B	Diode (CP301)	[BD1A]
72	VHDRB160L-401	AG		B	Diode (RB160L-40)	[D2,9A,10A,11A,12]
73	VHEMTZ5.1A/-1	AC		B	Zener diode (MTZ5.1A)	[ZD1A]
74	VHEPTZ30B++-1	AG	N	B	Zener diode (PTZ30B)	[ZD2A]
75	VHEPTZ5.6B/-1	AG		B	Zener diode (PTZ5.6B)	[ZD3A]
76	VHEUDZ33B//-1	AC		B	Zener diode (32.15-33.79)(UDZ33B)	[ZD4A,5A]
77	VHi2032ARAB1A	AZ		B	IC (ISPLS2032B1A)	[IC28]
78	VHi28F016SU70	BR		B	Flash memory (28F016SU70)	[IC35]
79	VHi4M16SŌJ60/	AV		B	DRAM (4M16SOJ60)	[IC37]
80	VHi51V8512T12	BG		B	4M PSRAM (TC51V8512AFT)	[IC33,34]
81	VHi74AHCT245D	AP		B	IC (74AHCT245NS)	[IC38]
82	VHi74LV08/DR/	AK		B	IC (74LV08)	[IC6]
83	VHi74LV138DR/	AP		B	IC (74LV138)	[IC48]
84	VHi74LV14ADR/	AM		B	IC (74LV14A)	[IC40]
85	VHi74LVX00/SJ	AL		B	IC (74LVX00)	[IC24,25]
86	VHi74LVX08/SJ	AG		B	IC (74LVX08)	[IC26]
87	VHi74LVX32/SJ	AL		B	IC (74LVX32)	[IC22,23]
88	VHiBA10339F-1	AD		B	IC (BA10339F)	[IC36A]
89	VHiBA10393F-1	AC		B	IC (BA10393F)	[IC15A]
90	VHiBR6265BF10	AR		B	IC (BR6265BF10)	[IC1]
91	VHiH6415108 10	BA		B	CPU (H641510810)	[IC30]
92	VHiKiA7045F-1	AL	N	B	IC (KIA7045)	[IC16A]
93	VHiKiA7806P-1	AK		B	IC (KIA7806P)	[IC9]
94	VHiL4960V//-1	AS		B	IC (L4960H)(ST TYPE)	[IC18A,19A]
95	VHiLZ9FK13/-1	BA		B	IC (MPCA8)(LZ9FK13)	[IC17]
96	VHiLZ9FT18/-1	AZ		B	IC (OPC2)(LZ9FT18)	[IC10]
97	VHi27256RDH1A	AW		B	EP ROM (27256RDH1A)	[IC8]
98	VHiMB62H149-1	BC		B	IC (MB62H149)	[IC11]
99	VHiMC145406F1	AL		B	IC (MC145406F)(VHIMC145406F-)	[IC2,4]
100	VHiMC68B54/-1	BB		B	IC (MC6BB54P)	[IC21]
101	VHiMN89303/-1	BD		B	IC (MN890303)	[IC29]
102	VHiRH5RE33A-1	AF		B	IC (RX5RE)	[IC49]
103	VHiSN74HC00DR	AG		B	IC (74HC00)	[IC12]
	VHiSN74HC00DR	AG		B	IC (74HC00)	[IC39,41]
104	VHiSN74HC04DR	AG		B	IC (SN74HC04DR)	[IC44]
105	VHiSN74HC08DR	AL		B	IC (SN74HC08DR D014 TAPPING)	[IC45]
106	VHiSN74HC74D1	AG		B	IC (SN74HC74)	[IC13]
107	VHiSN74HCU04D	AG		B	IC (SN74HCU04)	[IC42]
108	VHiSN75115NS1	AN		B	IC (SN75115NS1)	[IC5]
109	VHiSN75189DR/	AK		B	IC (SN75189DR)	[IC3]
110	VHiTA79L024-1	AE	N	B	Regurator IC (TA79L24BP)	[IC58A]
111	VHiTD62308F-1	AH		B	IC (TD62308F)	[IC7]
112	VHiUPD71037GB	AY		B	IC (UPD71037GB)	[IC43]
113	VHiZ84C0006FE	AT		B	IC (Z80-CPU)(Z84C0006FE)	[IC14]
114	VHiZ84C3006FE	AT		B	IC (Z80-CTC)(Z84C3006FE)	[IC20]
115	VHViCPS1.0/-1	AF		B	IC protector (ICPS1.0)	[ICP1]
116	VRD-RC2EY221J	AA		C	Resistor (1/4W 220Ω ±5%)	[R2]
117	VRS-RE3AAR39J	AB		C	Resistor (1W 0.39Ω ±5%)	[R5A]
118	VRS-RE3LA151J	AC		C	Resistor (3.0W 150Ω ±5%)	[R1]
119	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[R3]
	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[R9,64,121,128,163,204]
120	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R143,144,146,147,152,153,154,158]
	VRS-TS2AD101J	AA		C	Resistor (1/10W 100Ω ±5%)	[R159,160,166,167,168,174,175,176]
121	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R10,43,62,122A,125,203]
122	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R6,12,14,15,16,17,18,20,21,22]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R23,28,29,30,31,32,33,34,35,36]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R37,38,39,40,48,49,51,52,53,54]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R55,56,57,58,59,60,61,63,65,66]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R67,68,69,71,74,76,77,78,80,81]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R84,85,87,89,90,92,94,97,98,100]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R102,103,107,109,110,115,116,117]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R118,119,120,132,133,137,139,140]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R141,148,150,156,164,172,178,180]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R186,187,188,189,190,191,192,193]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R194,195,196,197,198,199,200,201]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R202,205,206,207,208,210,211,212]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R213,214,215,216,217,218,219,220]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R221,222,225,226,227,228,230,231]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
122	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R232,233,234,235,241A,245A]
123	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R237A]
124	VRS-TS2AD105J	AA		C	Resistor (1/10W 1MΩ ±5%) [R50,75]
125	VRS-TS2AD112J	AA		C	Resistor (1/10W 1.1KΩ ±5%) [R242A]
126	VRS-TS2AD122J	AA		C	Resistor (1/10W 1.2KΩ ±5%) [R41,247]
127	VRS-TS2AD123J	AA		C	Resistor (1/10W 12KΩ ±5%) [R25]
128	VRS-TS2AD143F	AB		C	Resistor (1/10W 14KΩ ±1%) [R101A]
129	VRS-TS2AD152G	AA		C	Resistor (1/10W 1.5KΩ ±2%) [R27,229A,236A]
130	VRS-TS2AD153G	AA		C	Resistor (1/10W 15KΩ ±2%) [R13,82A,93A,112A,182,243]
131	VRS-TS2AD162J	AA		C	Resistor (1/10W 1.6KΩ ±5%) [R24,26]
132	VRS-TS2AD222J	AA		C	Resistor (1/10W 2.2KΩ ±5%) [R8]
133	VRS-TS2AD272J	AA		C	Resistor (1/10W 2.7KΩ ±5%) [R73A,88A]
134	VRS-TS2AD302J	AA		C	Resistor (1/10W 3.0KΩ ±5%) [R70,91]
135	VRS-TS2AD303F	AA		C	Resistor (1/10W 30KΩ ±1%) [R224A]
136	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R124,126,127,129,131,134,135,162]
	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R169,177,184,185]
137	VRS-TS2AD392G	AA		C	Resistor (1/10W 3.9KΩ ±2%) [R42]
138	VRS-TS2AD432J	AA		C	Resistor (1/10W 4.3KΩ ±5%) [R105A,113A,238A]
139	VRS-TS2AD470J	AA		C	Resistor (1/10W 47Ω ±5%) [R138,151,157,165,173,179]
140	VRS-TS2AD472F	AA		C	Resistor (1/10W 4.7KΩ ±1%) [R96A]
141	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R7,45,46,47,95,99,104,108,111]
	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R114]
142	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%) [R11,181,183]
143	VRS-TS2AD512F	AA		C	Resistor (1/10W 5.1KΩ ±1%) [R223A]
144	VRS-TS2AD513J	AA		C	Resistor (1/10W 51KΩ ±5%) [R240A]
145	VRS-TS2AD561J	AA		C	Resistor (1/10W 560Ω ±5%) [R19]
146	VRS-TS2AD562J	AA		C	Resistor (1/10W 5.6KΩ ±5%) [R123A]
147	VRS-TS2AD563J	AA		C	Resistor (1/10W 56KΩ ±5%) [R83A]
148	VRS-TS2AD622F	AA		C	Resistor (1/10W 6.2KΩ ±1%)(VRS-TS2AD622G) [R79A,239A]
149	VRS-TS2AD681J	AA		C	Resistor (1/10W 680Ω ±5%) [R72]
150	VRS-TS2AD912G	AA		C	Resistor (1/10W 9.1KΩ ±2%) [R86A]
151	VRS-TS2HD122J	AC		C	Resistor (1/2W 1.2KΩ ±5%) [R161]
152	VRS-TS2HD130J	AD		C	Resistor (1/2W 13Ω ±5%) [R244,246]
153	VS2SA1270-/-1	AF		B	Transistor (2SA1270) [Q1A]
154	VS2SC4699KP-1	AC		B	Transistor (2SC4699YK) [Q8,9]
155	VS2SJ187-//-1	AF		B	Transistor (2SJ187) [Q7]
156	VSDTA144EK/-1	AC		B	Digital transistor (DTA144EK) [Q3]
157	VSDTC114YK/-1	AC		B	Transistor (DTC114YK) [Q2]
158	VSKTA1273//-1	AF		B	Transistor (KTA1273Y)(VSKTA1273Y/-1) [Q4]
159	VSKTC3199//-1	AC	N	B	Transistor (KTC3199GR)(VSKTC3199GR-1) [Q5]
160	VSKTD1413++-1	AN	N	B	Transistor (KTD1413) [Q6A]
161	XBPSD30P06000	AA		C	Screw (M3×6)
	(Unit)				
901	CPWBX2869BH01	CX	N	E	Main PWB unit

5 Mother PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM7203RC8J	AN		C	OPTION Connector (20-5061-080) [CN12]
2	QCNCW7204RC8J	AM		C	I/O Connector (80pin)(10-5061-080) [CN10,11]
3	VCEAEU1VW476M	AB		C	Capacitor (35WV 47μF) [C1]
	(Unit)				
901	CPWBX2868BH01	BL	N	E	Mother PWB unit

6 CKDC PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM5091BC1B	AD		C	Connector (MLX 5597-12CPB) [CON2]
2	QCNCM7127BH0H	AF		C	Connector (MLX 53048-0810) [CON7]
3	QCNCM7136BHZZ	AB		C	Connector (MLX 5229-13APB) [CON1]
4	QCNCM7142BH1B	AD		C	Connector (GIL-G12P-5ST2-E) [CON6]
5	QCNCW7207RC1H	AL		C	CKDC connector (MLX5597-18CPB) [CON4]
6	RALMB6640RCZZ	AF		B	Buzzer (SMX06) [BZ1]
7	RCiLZ5017SCZ/	AF		C	Chip core (BLM31) [FB10,11,12,13,14,15,16,17]
8	RCŌRF6691BHZZ	AD		C	Core (BFS3550R2F) [FB1,2,3,3,4,5,6,7,8]
9	RCRSP6676RCZZ	AG		B	Crystal (32.768KHz) [X1]
10	RCRSZ6644RCZZ	AD		B	Crystal (4.19MHz) [X2]
11	VCCCTV1HH150J	AA		C	Capacitor (50WV 15PF) [C8,9]
12	VCCCTV1HH471J	AA		C	Capacitor (50WV 470PF) [C4,5,6,7]
13	VCEAPS1CC106M	AC		C	Capacitor (16WV 10μF) [C2,12]
14	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C11]
15	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C3,16]

6 CKDC PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
16	VHD1SS353//-1	AB		B	Diode (1SS353) [D1,2,3,4,5,6,7,8,9,10,11,12,13]
	VHD1SS353//-1	AB		B	Diode (1SS353) [D14,15,19,20,21,22,23,24,26]
17	VHi74HC138DR/	AK		B	IC (SN74HC138DR) [IC1,2]
18	VHiH4728B02FS	AW		B	IC (CKDC9)(H4728B02FS) [IC8]
19	VHiSN74HC153D	AK		B	IC (SN74HC153DR) [IC5,4]
20	VHiSN74LS125R	AL		B	IC (SN74LS125DR) [IC3,6]
21	VRS-TS2AD105J	AA		C	Resistor (1/10W 1MΩ ±5%) [R33]
22	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R13,14,28]
23	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%) [R1,2,3,4,5,6,7,8,9,10,11,12,15]
	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%) [R16,17,18,19,20,21,22,23,24,25,26]
24	VSDTC114YK/-1	AC		B	Transistor (DTC114YK) [Q1]
	(Unit)				
901	CPWBN7511BH03	BR	N	E	CKDC PWB unit

7 N/F PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW7199BH0E	AE		C	Connector (35328-0510) [CN2A]
⚠ 2	QFS-D4341CCZZ	AE		A	Fuse (SEMCO T1A/250V)(QFS-D4341BHZZ) [F1A]
3	QFSHD2109AFZZ	AC		C	Fuse holder (HD2109AF) [F1A]
4	QSW-C1262QCZZ	AR		B	Power switch (AJ7241B) [SW1A]
5	QTANN6658RCZZ	AH		C	Block terminal [CN1A]
6	RC-FZ1041RC2E	AE		C	Capacitor (250WV 0.1μF) [C1A,2A]
7	RCiLC6654BHZZ	AR		C	Coil (5021C) [L1A]
8	VRD-RB2HY394J	AA		C	Resistor (1/2W 390KΩ ±5%) [R1A]
	(Unit)				
901	CPWBF2867BH01	BF	N	E	N/F PWB unit

8 Invertor PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM7179BH0D	AD		C	INV connector (MLX53015-0410) [CON3]
2	QCNCM7209RC1E	AL		C	LCD I/Fconnector (MLX 53048-1510) [CON1]
3	QCNCM7212RC0B	AC		C	CCFT connector (EH S2B) [CON4,6]
4	QCNCW7208RC1B	AG		C	LCD connector (MLX 52044-1245) [COM2]
5	RC-AZ1801RC0F	AE		C	Capacitor (3.15KV 18pF) [C1]
6	RC-FZ2241RC2A	AG		C	Capacitor (100WV 0.22μF) [C5]
7	RCiLC6659RCZZ	AR		C	Chock coil (D10F,A814AY-101K) [L1]
⚠ 8	RTRNH6896RCZZ	BA		B	D/A inverter transformer (841TN-1024) [T1]
9	VCEAPS1CC225M	AF		C	Capacitor (16WV 2.2μF) [C2,4]
10	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1μF) [C6]
11	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C3]
12	VHDSFPB54//-1	AC		B	Diode (SFPB54) [D1,2]
13	VHiLT1184CS-1	BE		B	IC (LT1184) [IC1]
14	VHViCPS0.5/-1	AF		B	IC-protector (ICPS0.5) [F1]
15	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R3]
16	VRS-TS2AD224J	AA		C	Resistor (1/10W 220KΩ ±5%) [R2]
17	VRS-TS2AD332F	AA		C	Resistor (1/10W 3.3KΩ ±1%) [R6]
18	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R1]
19	VRS-TS2AD751J	AA		C	Resistor (1/10W 750Ω ±5%) [R4]
20	VRS-TS2AD822G	AA	N	C	Resistor (1/10W 8.2KΩ ±2%) [R5]
21	VS2SC5001R/-1	AF		B	Transistor (2SC5001) [Q1,2]
	(Unit)				
901	CPWBN7512BH01	BQ		E	Inverter PWB unit

9 Service tools

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM7145RCZZ	AZ		S	Terminator [SRN in-line system]
2	UKŌG-6718RCZZ	BE		S	MCR test card [for UP-E12MR]
3	UKŌG-6705RCZZ	BC		S	RS-232 loop back connector [for RS-232 connector]
4	CKŌG-6724BHZZ	BQ		S	Extension PWB
5	LKGiM7377BH07	BA		S	1 hole clerk key (7)(2pcs/1set,with key ring)
6	LKGiM7377BH08	BA		S	1 hole clerk key (8)(2pcs/1set,with key ring)
7	LKGiM7377BH09	BA		S	1 hole clerk key (9)(2pcs/1set,with key ring)
8	LKGiM7377BH10	BA		S	1 hole clerk key (10)(2pcs/1set,with key ring)
9	LKGiM7377BH11	BA		S	1 hole clerk key (11)(2pcs/1set,with key ring)
10	LKGiM7377BH12	BA		S	1 hole clerk key (12)(2pcs/1set,with key ring)

9 Service tools

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
11	LKGiM7377BH13	BA		S	1 hole clerk key (13)(2pcs/1set,with key ring)
12	LKGiM7377BH14	BA		S	1 hole clerk key (14)(2pcs/1set,with key ring)
13	LKGiM7377BH15	BA		S	1 hole clerk key (16)(2pcs/1set,with key ring)
14	LKGiM7377BH16	BA		S	1 hole clerk key (15)(2pcs/1set,with key ring)
15	LKGiM7377BH17	BA		S	1 hole clerk key (17)(2pcs/1set,with key ring)
16	LKGiM7377BH18	BA		S	1 hole clerk key (18)(2pcs/1set,with key ring)
17	LKGiM7377BH19	BA		S	1 hole clerk key (19)(2pcs/1set,with key ring)
18	LKGiM7377BH20	BA		S	1 hole clerk key (20)(2pcs/1set,with key ring)
19	LKGiM7377BH21	BA		S	1 hole clerk key (21)(2pcs/1set,with key ring)
20	LKGiM7377BH22	BA		S	1 hole clerk key (22)(2pcs/1set,with key ring)
21	LKGiM7377BH23	BA		S	1 hole clerk key (23)(2pcs/1set,with key ring)
22	LKGiM7377BH24	BA		S	1 hole clerk key (24)(2pcs/1set,with key ring)
23	LKGiM7377BH25	BA		S	1 hole clerk key (25)(2pcs/1set,with key ring)
24	LKGiM7377BH26	BA		S	1 hole clerk key (26)(2pcs/1set,with key ring)
25	LKGiM7377BH27	BA		S	1 hole clerk key (27)(2pcs/1set,with key ring)
26	LKGiM7377BH28	BA		S	1 hole clerk key (28)(2pcs/1set,with key ring)
27	LKGiM7377BH29	BA		S	1 hole clerk key (29)(2pcs/1set,with key ring)
28	LKGiM7377BH30	BA		S	1 hole clerk key (30)(2pcs/1set,with key ring)
29	LKGiM7377BH31	BA		S	1 hole clerk key (31)(2pcs/1set,with key ring)
30	LKGiM7377BH32	BA		S	1 hole clerk key (32)(2pcs/1set,with key ring)
31	LKGiM7377BH33	BA		S	1 hole clerk key (33)(2pcs/1set,with key ring)
32	LKGiM7377BH34	BA		S	1 hole clerk key (34)(2pcs/1set,with key ring)
33	LKGiM7377BH35	BA		S	1 hole clerk key (35)(2pcs/1set,with key ring)
34	LKGiM7377BH36	BA		S	1 hole clerk key (36)(2pcs/1set,with key ring)
35	LKGiM7377BH37	BA		S	1 hole clerk key (37)(2pcs/1set,with key ring)
36	LKGiM7377BH38	BA		S	1 hole clerk key (38)(2pcs/1set,with key ring)
37	LKGiM7377BH39	BA		S	1 hole clerk key (39)(2pcs/1set,with key ring)
38	LKGiM7377BH40	BA		S	1 hole clerk key (40)(2pcs/1set,with key ring)
39	LKGiM7377BH41	BA		S	1 hole clerk key (41)(2pcs/1set,with key ring)
40	LKGiM7377BH42	BA		S	1 hole clerk key (42)(2pcs/1set,with key ring)
41	LKGiM7377BH43	BA		S	1 hole clerk key (43)(2pcs/1set,with key ring)
42	LKGiM7377BH44	BA		S	1 hole clerk key (44)(2pcs/1set,with key ring)
43	LKGiM7377BH45	BA		S	1 hole clerk key (45)(2pcs/1set,with key ring)
44	LKGiM7377BH46	BA		S	1 hole clerk key (46)(2pcs/1set,with key ring)
45	LKGiM7377BH47	BA		S	1 hole clerk key (47)(2pcs/1set,with key ring)
46	LKGiM7377BH48	BA		S	1 hole clerk key (48)(2pcs/1set,with key ring)
47	LKGiM7377BH49	BA		S	1 hole clerk key (49)(2pcs/1set,with key ring)
48	LKGiM7377BH50	BA		S	1 hole clerk key (50)(2pcs/1set,with key ring)
49	LKGiM7377BH51	BA		S	1 hole clerk key (51)(2pcs/1set,with key ring)
50	LKGiM7377BH52	BA		S	1 hole clerk key (52)(2pcs/1set,with key ring)
51	LKGiM7377BH53	BA		S	1 hole clerk key (53)(2pcs/1set,with key ring)
52	LKGiM7377BH54	BA		S	1 hole clerk key (54)(2pcs/1set,with key ring)
53	LKGiM7377BH55	BA		S	1 hole clerk key (55)(2pcs/1set,with key ring)
54	LKGiM7377BH56	BA		S	1 hole clerk key (56)(2pcs/1set,with key ring)
55	LKGiM7377BH57	BA		S	1 hole clerk key (57)(2pcs/1set,with key ring)
56	LKGiM7377BH58	BA		S	1 hole clerk key (58)(2pcs/1set,with key ring)
57	LKGiM7377BH59	BA		S	1 hole clerk key (59)(2pcs/1set,with key ring)
58	LKGiM7377BH60	BA		S	1 hole clerk key (60)(2pcs/1set,with key ring)
59	LKGiM7377BH61	BA		S	1 hole clerk key (61)(2pcs/1set,with key ring)
60	LKGiM7377BH62	BA		S	1 hole clerk key (62)(2pcs/1set,with key ring)
61	LKGiM7377BH63	BA		S	1 hole clerk key (63)(2pcs/1set,with key ring)
62	LKGiM7377BH64	BA		S	1 hole clerk key (64)(2pcs/1set,with key ring)
63	LKGiM7377BH65	BA		S	1 hole clerk key (65)(2pcs/1set,with key ring)
64	LKGiM7377BH66	BA		S	1 hole clerk key (66)(2pcs/1set,with key ring)
65	LKGiM7377BH67	BA		S	1 hole clerk key (67)(2pcs/1set,with key ring)
66	LKGiM7377BH68	BA		S	1 hole clerk key (68)(2pcs/1set,with key ring)
67	LKGiM7377BH69	BA		S	1 hole clerk key (69)(2pcs/1set,with key ring)
68	LKGiM7377BH70	BA		S	1 hole clerk key (70)(2pcs/1set,with key ring)
69	LKGiM7377BH71	BA		S	1 hole clerk key (71)(2pcs/1set,with key ring)
70	LKGiM7377BH72	BA		S	1 hole clerk key (72)(2pcs/1set,with key ring)
71	LKGiM7377BH73	BA		S	1 hole clerk key (73)(2pcs/1set,with key ring)
72	LKGiM7377BH74	BA		S	1 hole clerk key (74)(2pcs/1set,with key ring)
73	LKGiM7377BH75	BA		S	1 hole clerk key (75)(2pcs/1set,with key ring)
74	LKGiM7377BH76	BA		S	1 hole clerk key (76)(2pcs/1set,with key ring)
75	LKGiM7377BH77	BA		S	1 hole clerk key (77)(2pcs/1set,with key ring)
76	LKGiM7377BH78	BA		S	1 hole clerk key (78)(2pcs/1set,with key ring)
77	LKGiM7377BH79	BA		S	1 hole clerk key (79)(2pcs/1set,with key ring)
78	LKGiM7377BH80	BA		S	1 hole clerk key (80)(2pcs/1set,with key ring)
79	LKGiM7377BH81	BA		S	1 hole clerk key (81)(2pcs/1set,with key ring)
80	LKGiM7377BH82	BA		S	1 hole clerk key (82)(2pcs/1set,with key ring)
81	LKGiM7377BH83	BA		S	1 hole clerk key (83)(2pcs/1set,with key ring)
82	LKGiM7377BH84	BA		S	1 hole clerk key (84)(2pcs/1set,with key ring)
83	LKGiM7377BH85	BA		S	1 hole clerk key (85)(2pcs/1set,with key ring)
84	LKGiM7377BH86	BA		S	1 hole clerk key (86)(2pcs/1set,with key ring)
85	LKGiM7377BH87	BA		S	1 hole clerk key (87)(2pcs/1set,with key ring)
86	LKGiM7377BH88	BA		S	1 hole clerk key (88)(2pcs/1set,with key ring)
87	LKGiM7377BH89	BA		S	1 hole clerk key (89)(2pcs/1set,with key ring)
88	LKGiM7377BH90	BA		S	1 hole clerk key (90)(2pcs/1set,with key ring)
89	LKGiM7377BH91	BA		S	1 hole clerk key (91)(2pcs/1set,with key ring)
90	LKGiM7377BH92	BA		S	1 hole clerk key (92)(2pcs/1set,with key ring)

9 Service tools

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
91	LKGiM7377BH93	BA		S	1 hole clerk key (93)(2pcs/1set,with key ring)
92	LKGiM7377BH94	BA		S	1 hole clerk key (94)(2pcs/1set,with key ring)
93	LKGiM7377BH95	BA		S	1 hole clerk key (95)(2pcs/1set,with key ring)
94	LKGiM7377BH96	BA		S	1 hole clerk key (96)(2pcs/1set,with key ring)
95	LKGiM7377BH97	BA		S	1 hole clerk key (97)(2pcs/1set,with key ring)
96	LKGiM7377BH98	BA		S	1 hole clerk key (98)(2pcs/1set,with key ring)
97	LKGiM7377BH99	BA		S	1 hole clerk key (99)(2pcs/1set,with key ring)
98	LKGiM7377BH00	BA		S	1 hole clerk key (100)(2pcs/1set,with key ring)
99	LKGiM7377BHA1	BA		S	1 hole clerk key (101)(2pcs/1set,with key ring)
100	LKGiM7377BHA2	BA		S	1 hole clerk key (102)(2pcs/1set,with key ring)
101	LKGiM7377BHA3	BA		S	1 hole clerk key (103)(2pcs/1set,with key ring)
102	LKGiM7377BHA4	BA		S	1 hole clerk key (104)(2pcs/1set,with key ring)
103	LKGiM7377BHA5	BA		S	1 hole clerk key (105)(2pcs/1set,with key ring)
104	LKGiM7377BHA6	BA		S	1 hole clerk key (106)(2pcs/1set,with key ring)
105	LKGiM7377BHA7	BA		S	1 hole clerk key (107)(2pcs/1set,with key ring)
106	LKGiM7377BHA8	BA		S	1 hole clerk key (108)(2pcs/1set,with key ring)
107	LKGiM7377BHA9	BA		S	1 hole clerk key (109)(2pcs/1set,with key ring)
108	LKGiM7377BHA0	BA		S	1 hole clerk key (110)(2pcs/1set,with key ring)
109	LKGiM7377BHB1	BA		S	1 hole clerk key (111)(2pcs/1set,with key ring)
110	LKGiM7377BHB2	BA		S	1 hole clerk key (112)(2pcs/1set,with key ring)
111	LKGiM7377BHB3	BA		S	1 hole clerk key (113)(2pcs/1set,with key ring)
112	LKGiM7377BHB4	BA		S	1 hole clerk key (114)(2pcs/1set,with key ring)
113	LKGiM7377BHB5	BA		S	1 hole clerk key (115)(2pcs/1set,with key ring)
114	LKGiM7377BHB6	BA		S	1 hole clerk key (116)(2pcs/1set,with key ring)
115	LKGiM7377BHB7	BA		S	1 hole clerk key (117)(2pcs/1set,with key ring)
116	LKGiM7377BHB8	BA		S	1 hole clerk key (118)(2pcs/1set,with key ring)
117	LKGiM7377BHB9	BA		S	1 hole clerk key (119)(2pcs/1set,with key ring)
118	LKGiM7377BHB0	BA		S	1 hole clerk key (120)(2pcs/1set,with key ring)
119	LKGiM7377BHC1	BA		S	1 hole clerk key (121)(2pcs/1set,with key ring)
120	LKGiM7377BHC2	BA		S	1 hole clerk key (122)(2pcs/1set,with key ring)
121	LKGiM7377BHC3	BA		S	1 hole clerk key (123)(2pcs/1set,with key ring)
122	LKGiM7377BHC4	BA		S	1 hole clerk key (124)(2pcs/1set,with key ring)
123	LKGiM7377BHC5	BA		S	1 hole clerk key (125)(2pcs/1set,with key ring)
124	LKGiM7377BHC6	BA		S	1 hole clerk key (126)(2pcs/1set,with key ring)

10 Supply

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	PSHEK6818BHZZ	AQ		S	Blank key sheet

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
【C】					
CKŌG-6724BHZZ	9- 4	BQ		S	
CPWBF2867BH01	2- 17	BF	N	E	
〃	7-901	BF	N	E	
CPWBN7511BH03	1- 22	BR	N	E	
〃	6-901	BR	N	E	
CPWBN7512BH01	1- 21	BQ		E	
〃	8-901	BQ		E	
CPWBX2868BH01	2- 7	BL	N	E	
〃	5-901	BL	N	E	
CPWBX2869BH01	2- 22	CX	N	E	
〃	4-901	CX	N	E	
CSHEP6817BH01	1- 11	BB		C	
【D】					
DUNTK4783BHZZ	1-501	BN		E	
【G】					
GCABA7205BHZA	2- 32	BH	N	D	
GCABB7202BHSC	1- 3	BF	N	D	
GCABF2551BHZZ	1- 45	AY	N	D	
GCABR7256BHSA	1- 36	AZ	N	D	
GCŌVA7080BHSC	1- 1	AR	N	D	
GCŌVA7085BHZA	2- 25	BB	N	D	
GCŌVA7086BHZA	2- 26	AZ	N	D	
GCŌVB2503BHZZ	1- 2	BR	N	D	
GCŌVB7082BHZZ	1- 8	AZ		D	
GCŌVH7133BHZZ	1- 23	AH		D	
GCŌVH7150BHZZ	2- 41	AR		D	
GFTAB6788BHSD	2- 39	AN	N	D	
GFTAS6787BHSC	2- 42	AM	N	D	
GFTAS6789BHSC	2- 27	AH	N	D	
GFTAS6790BHSC	2- 24	AH	N	D	
GFTAS6927BHSA	2- 35	AM	N	D	
GLEGG6656BHZZ	2- 37	AF		D	
GLEGG6659BHZZ	2- 45	AE		D	
GLEGP6657BHSA	2- 44	AM		D	
GLEGP6658BHSA	2- 43	AL		D	
【H】					
HDECP2369BHZZ	1- 56	BA	N	D	
【L】					
LANGK2884BHZZ	2- 8	AS	N	C	
LANGK7561BHZZ	1- 31	AK		C	
LANGK7617BHZZ	2- 1	BA		C	
LANGK7618BHZZ	2- 5	AQ		C	
LANGQ7565BHZZ	1- 19	AE		C	
LANGT2885BHZZ	2- 61	AS	N	C	
LANGT2886BHZZ	2- 10	AU	N	C	
LANGT7559BHZZ	1- 15	AW		C	
LANGT7607BHZB	2- 6	AT	N	C	
LBNDJ2003SCZZ	2- 20	AA		C	
LCHSM6707BHZZ	2- 40	AN		C	
LCHSM6708BHZA	2- 49	AR	N	C	
LFRM-6691BHZZ	1- 9	AZ		D	
LHLDW0008SCZZ	1- 58	AA		C	
LHLDW6843BHZZ	1- 49	AE		C	
〃	2- 54	AE		C	
LKGiM7377BH00	9- 98	BA		S	
LKGiM7377BH01	1- 18	AV		B	
〃	3- 11	AV		B	
LKGiM7377BH02	1- 18	AV		B	
〃	3- 11	AV		B	
LKGiM7377BH03	1- 18	AV		B	
〃	3- 11	AV		B	
LKGiM7377BH04	1- 18	AV		B	
〃	3- 11	AV		B	
LKGiM7377BH05	1- 18	AV		B	
〃	3- 11	AV		B	
LKGiM7377BH06	1- 18	AV		B	
〃	3- 11	AV		B	
LKGiM7377BH07	9- 5	BA		S	
LKGiM7377BH08	9- 6	BA		S	
LKGiM7377BH09	9- 7	BA		S	
LKGiM7377BH10	9- 8	BA		S	
LKGiM7377BH11	9- 9	BA		S	
LKGiM7377BH12	9- 10	BA		S	
LKGiM7377BH13	9- 11	BA		S	
LKGiM7377BH14	9- 12	BA		S	
LKGiM7377BH15	9- 13	BA		S	
LKGiM7377BH16	9- 14	BA		S	
LKGiM7377BH17	9- 15	BA		S	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
LKGiM7377BH18	9- 16	BA		S	
LKGiM7377BH19	9- 17	BA		S	
LKGiM7377BH20	9- 18	BA		S	
LKGiM7377BH21	9- 19	BA		S	
LKGiM7377BH22	9- 20	BA		S	
LKGiM7377BH23	9- 21	BA		S	
LKGiM7377BH24	9- 22	BA		S	
LKGiM7377BH25	9- 23	BA		S	
LKGiM7377BH26	9- 24	BA		S	
LKGiM7377BH27	9- 25	BA		S	
LKGiM7377BH28	9- 26	BA		S	
LKGiM7377BH29	9- 27	BA		S	
LKGiM7377BH30	9- 28	BA		S	
LKGiM7377BH31	9- 29	BA		S	
LKGiM7377BH32	9- 30	BA		S	
LKGiM7377BH33	9- 31	BA		S	
LKGiM7377BH34	9- 32	BA		S	
LKGiM7377BH35	9- 33	BA		S	
LKGiM7377BH36	9- 34	BA		S	
LKGiM7377BH37	9- 35	BA		S	
LKGiM7377BH38	9- 36	BA		S	
LKGiM7377BH39	9- 37	BA		S	
LKGiM7377BH40	9- 38	BA		S	
LKGiM7377BH41	9- 39	BA		S	
LKGiM7377BH42	9- 40	BA		S	
LKGiM7377BH43	9- 41	BA		S	
LKGiM7377BH44	9- 42	BA		S	
LKGiM7377BH45	9- 43	BA		S	
LKGiM7377BH46	9- 44	BA		S	
LKGiM7377BH47	9- 45	BA		S	
LKGiM7377BH48	9- 46	BA		S	
LKGiM7377BH49	9- 47	BA		S	
LKGiM7377BH50	9- 48	BA		S	
LKGiM7377BH51	9- 49	BA		S	
LKGiM7377BH52	9- 50	BA		S	
LKGiM7377BH53	9- 51	BA		S	
LKGiM7377BH54	9- 52	BA		S	
LKGiM7377BH55	9- 53	BA		S	
LKGiM7377BH56	9- 54	BA		S	
LKGiM7377BH57	9- 55	BA		S	
LKGiM7377BH58	9- 56	BA		S	
LKGiM7377BH59	9- 57	BA		S	
LKGiM7377BH60	9- 58	BA		S	
LKGiM7377BH61	9- 59	BA		S	
LKGiM7377BH62	9- 60	BA		S	
LKGiM7377BH63	9- 61	BA		S	
LKGiM7377BH64	9- 62	BA		S	
LKGiM7377BH65	9- 63	BA		S	
LKGiM7377BH66	9- 64	BA		S	
LKGiM7377BH67	9- 65	BA		S	
LKGiM7377BH68	9- 66	BA		S	
LKGiM7377BH69	9- 67	BA		S	
LKGiM7377BH70	9- 68	BA		S	
LKGiM7377BH71	9- 69	BA		S	
LKGiM7377BH72	9- 70	BA		S	
LKGiM7377BH73	9- 71	BA		S	
LKGiM7377BH74	9- 72	BA		S	
LKGiM7377BH75	9- 73	BA		S	
LKGiM7377BH76	9- 74	BA		S	
LKGiM7377BH77	9- 75	BA		S	
LKGiM7377BH78	9- 76	BA		S	
LKGiM7377BH79	9- 77	BA		S	
LKGiM7377BH80	9- 78	BA		S	
LKGiM7377BH81	9- 79	BA		S	
LKGiM7377BH82	9- 80	BA		S	
LKGiM7377BH83	9- 81	BA		S	
LKGiM7377BH84	9- 82	BA		S	
LKGiM7377BH85	9- 83	BA		S	
LKGiM7377BH86	9- 84	BA		S	
LKGiM7377BH87	9- 85	BA		S	
LKGiM7377BH88	9- 86	BA		S	
LKGiM7377BH89	9- 87	BA		S	
LKGiM7377BH90	9- 88	BA		S	
LKGiM7377BH91	9- 89	BA		S	
LKGiM7377BH92	9- 90	BA		S	
LKGiM7377BH93	9- 91	BA		S	
LKGiM7377BH94	9- 92	BA		S	
LKGiM7377BH95	9- 93	BA		S	
LKGiM7377BH96	9- 94	BA		S	
LKGiM7377BH97	9- 95	BA		S	
LKGiM7377BH98	9- 96	BA		S	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
LKGiM7377BH99	9- 97	BA		S	
LKGiM7377BHA0	9-108	BA		S	
LKGiM7377BHA1	9- 99	BA		S	
LKGiM7377BHA2	9-100	BA		S	
LKGiM7377BHA3	9-101	BA		S	
LKGiM7377BHA4	9-102	BA		S	
LKGiM7377BHA5	9-103	BA		S	
LKGiM7377BHA6	9-104	BA		S	
LKGiM7377BHA7	9-105	BA		S	
LKGiM7377BHA8	9-106	BA		S	
LKGiM7377BHA9	9-107	BA		S	
LKGiM7377BHB0	9-118	BA		S	
LKGiM7377BHB1	9-109	BA		S	
LKGiM7377BHB2	9-110	BA		S	
LKGiM7377BHB3	9-111	BA		S	
LKGiM7377BHB4	9-112	BA		S	
LKGiM7377BHB5	9-113	BA		S	
LKGiM7377BHB6	9-114	BA		S	
LKGiM7377BHB7	9-115	BA		S	
LKGiM7377BHB8	9-116	BA		S	
LKGiM7377BHB9	9-117	BA		S	
LKGiM7377BHC1	9-119	BA		S	
LKGiM7377BHC2	9-120	BA		S	
LKGiM7377BHC3	9-121	BA		S	
LKGiM7377BHC4	9-122	BA		S	
LKGiM7377BHC5	9-123	BA		S	
LKGiM7377BHC6	9-124	BA		S	
LKGiW7375BHZZ	1- 16	BG		B	
LPLTM6693BHZZ	1- 12	AX		C	
LPLTM6714BHZZ	1- 37	AV		C	
LX-BZ6644BHZZ	4- 1	AA		C	
LX-BZ6781BHZZ	2- 16	AB		C	
LX-BZ6782BHZZ	1- 20	AA		C	
〃	2- 4	AA		C	
LX-BZ6792BHZZ	2- 30	AF		C	
【M】					
MHNG-6637BHZZ	1- 6	AU		C	
MHNG-6638BHZZ	1- 4	AU		C	
【P】					
PGUMM6712BHZZ	1- 10	BG		C	
PRDAF2379BHZZ	4- 2	AS	N	C	
PSHEK2904BHZZ	1- 25	AT	N	C	
PSHEK6818BHZZ	1- 7	AQ		C	
〃	10- 1	AQ		S	
PSHEK6852BHZZ	1- 26	AT		C	
PSHEP2902BHZZ	2- 58	AK	N	C	
PSHEP2907BHZZ	2- 60	AP	N	C	
PSHEP2918BHZZ	2- 52	AK	N	C	
PSHEP6853BHZZ	2- 48	AG		C	
【Q】					
QACCL7421BHZZ	2- 33	AX		B	
QACCV6422BHZZ	2- 33	AY		B	
QCNCM1060AC03	4- 3	AB		C	
QCNCM1101BHZZ	4- 4	AC		C	
QCNCM2551RC1J	4- 5	AF		C	
QCNCM5091BC1B	6- 1	AD		C	
QCNCM5278NCZZ	4- 6	AC		C	
QCNCM7057BH08	4- 7	AG		C	
QCNCM7075BH0B	4- 8	AB		C	
QCNCM7127BH0H	6- 2	AF		C	
QCNCM7128BH1E	4- 9	AH		C	
QCNCM7129BH0D	4- 10	AB		C	
QCNCM7136BHZZ	6- 3	AB		C	
QCNCM7142BH1B	6- 4	AD		C	
QCNCM7145RCZZ	9- 1	AZ		S	
QCNCM7179BH0D	8- 1	AD		C	
QCNCM7203RC8J	5- 1	AN		C	
QCNCM7209RC1E	8- 2	AL		C	
QCNCM7212RC0B	8- 3	AC		C	
QCNCM7222BH0i	4- 11	AD		C	
QCNCW1057ACZZ	4- 12	AB		C	
QCNCW7081BHZZ	4- 13	AB		C	
QCNCW7199BH0E	7- 1	AE		C	
QCNCW7204RC8J	4- 14	AM		C	
〃	5- 2	AM		C	
QCNCW7206RC1H	4- 15	AG		C	
QCNCW7207RC1H	6- 5	AL		C	
QCNCW7208RC1B	8- 4	AG		C	
QCNW-3051BHZZ	1- 50	AE	N	C	
QCNW-3052BHZZ	2- 29	AF		C	
QCNW-3091BHZZ	2- 21	AN	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
QCNW-7212RCZZ	2- 33	AH		B	
QCNW-7828BHZZ	1- 39	BC		C	
QCNW-7829BHZZ	1- 32	AP		C	
QCNW-7830BHZZ	1- 24	AQ		C	
QCNW-7832BHZZ	1- 34	AF		C	
QCNW-7871BHZZ	2- 31	BC		C	
QFS-C1035CCZZ	4- 16	AE		A	
QFS-C5012BHZZ	4- 17	AF		A	
QFS-D4341CCZZ	7- 2	AE		A	
QFSHD2109AFZZ	4- 18	AC		C	
〃	7- 3	AC		C	
QSŌCZ1012AC7B	4- 19	AP		C	
QSŌCZ6428ACZZ	4- 20	AE		C	
QSW-C1262QCZZ	7- 4	AR		B	
QSW-S0744AFZZ	4- 21	AG		B	
QSW-S6894BHZZ	4- 22	AK		B	
QTANN6658RCZZ	7- 5	AH		C	
QTANP0004BHZA	2- 57	AE		C	
QTANZ6661BHZZ	2- 14	AE		C	
【R】					
RALMB6640RCZZ	6- 6	AF		B	
RC-AZ1801RC0F	8- 5	AE		C	
RC-EZ106ARC1A	4- 23	AD		C	
RC-EZ2271RC1A	4- 24	AM		C	
RC-EZ336ARC1A	4- 25	AB		C	
RC-FZ1041RC2E	7- 6	AE		C	
RC-FZ2241RC2A	8- 6	AG		C	
RCiLC2421BHZZ	4- 26	AP	N	C	
RCiLC2422BHZZ	4- 27	AP	N	C	
RCiLC6654BHZZ	7- 7	AR		C	
RCiLC6659RCZZ	8- 7	AR		C	
RCiLZ5017SCZ/	4- 28	AF		C	
〃	6- 7	AF		C	
RCŌRF1008ACZZ	4- 29	AB		C	
RCŌRF2337BHZZ	4- 30	AN		C	
RCŌRF6691BHZZ	4- 31	AD		C	
〃	6- 8	AD		C	
RCŌRF6695BHZZ	1- 55	AK		C	
〃	2- 53	AK		C	
RCŌRF6697BHZZ	1- 27	AF		C	
〃	2- 55	AF		C	
RCŌRF6698BHZZ	1- 29	AR		C	
〃	2- 12	AR		C	
RCŌRF6699BHZZ	1- 57	AU		C	
〃	3- 13	AU		C	
RCŌRF6700BHZZ	3- 14	AS		C	
RCŌRF6702BHZZ	4- 32	AF		C	
RCŌRF6705BHZZ	2- 65	AM		C	
RCRMZ1016LCZZ	4- 33	AF		B	
RCRSP5019BCZZ	4- 34	AD		B	
RCRSP6664RCZZ	4- 35	AF		B	
RCRSP6676RCZZ	6- 9	AG		B	
RCRSZ2407RCZZ	4- 36	AQ	N	B	
RCRSZ6644RCZZ	6- 10	AD		B	
RMPTQ4330QCJJ	4- 37	AC		B	
RTRNH2419RCZZ	4- 38	AV	N	B	
RTRNH6896RCZZ	8- 8	BA		B	
RTRNP2416BHZZ	2- 19	BL	N	B	
RTRNP2417BHZZ	2- 19	BL	N	B	
RVR-B2410QCZZ	4- 39	AG		B	
RVR-M2415QCN3	4- 40	AE		B	
【S】					
SPAKA3129BHZZ	3- 7	AU		D	
SPAKA8409BHAL	3- 1	AX	N	D	
SPAKA8410BHAR	3- 3	AX	N	D	
SPAKA8435BHZZ	3- 5	AF		D	
SPAKC3132BHZZ	3- 4	BA	N	D	
SSAKA5004CCZZ	3- 10	AA		D	
SSAKH0003DHZZ	3- 2	AE		D	
SSAKH0013HCZZ	3- 8	AA		D	
SSAKH3015CCZZ	3- 8	AA		D	
SSAKH4231CCZZ	3- 6	AA		D	
【T】					
TCADH6788BHZA	3- 12	AC		D	
TCADZ2001BHZA	3- 17	AM		D	
TCAUS6677BHZZ	2- 47	AD		D	
TGANE1001BHZC	3- 16	AG		D	
TiNSE2407BHZZ	3- 9	BK	N	D	
TiNSE2411BHZZ	3- 9	BF	N	D	
TiNSE2420BHZZ	3- 9	BK	N	D	
TiNSE2421BHZZ	3- 9	BF	N	D	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
TiNSF2409BHZZ	3- 9	BK	N	D	
TiNSF2413BHZZ	3- 9	BF	N	D	
TiNSG2408BHZZ	3- 9	BK	N	D	
TiNSG2412BHZZ	3- 9	BF	N	D	
TiNSS2410BHZZ	3- 9	BK	N	D	
TiNSS2414BHZZ	3- 9	BF	N	D	
TLABG6967BHZZ	2- 46	AC		D	
TLABG7097BHZZ	2- 64	AF		D	
TLABH6996BHZZ	2- 63	AD		D	
TLABH7100BHSA	2- 23	AG	N	D	
TLABH7101BHZA	2- 59	AL		D	
TLABH7105BHSA	2- 51	AH	N	D	
【U】					
UBATN2338RCZZ	2- 38	BE		B	
UBNDA6629BHZZ	3- 15	AA		C	
UKŌG-6705RCZZ	9- 3	BC		S	
UKŌG-6718RCZZ	9- 2	BE		S	
【V】					
VCCCTV1HH100J	4- 41	AA		C	
VCCCTV1HH101J	4- 42	AA		C	
VCCCTV1HH150J	6- 11	AA		C	
VCCCTV1HH221J	4- 43	AA		C	
VCCCTV1HH331J	4- 44	AA		C	
VCCCTV1HH470J	4- 45	AA		C	
VCCCTV1HH471J	4- 46	AA		C	
〃	6- 12	AA		C	
VCCCTV1HH510J	4- 47	AA		C	
VCEAEU1CW106M	4- 48	AA		C	
VCEAEU1VW476M	4- 49	AB		C	
〃	5- 3	AB		C	
VCEAGA1HW104M	4- 50	AB		C	
VCEAGA1HW105M	4- 51	AB		C	
VCEAGA1HW106M	4- 52	AA		C	
VCEAGA1HW107M	4- 53	AA		C	
VCEAGA1HW224M	4- 54	AA		C	
VCEAGA1HW335M	4- 55	AB		C	
VCEAGD1CW108M	4- 56	AE		C	
VCEAGD1HW337M	4- 57	AF		C	
VCEAGU1HW108M	4- 58	AF		C	
VCEAGU1HW478M	4- 59	AL		C	
VCEAPS1CC106M	6- 13	AC		C	
VCEAPS1CC225M	8- 9	AF		C	
VCKYTV1CF105Z	4- 60	AB		C	
〃	8- 10	AB		C	
VCKYTV1HB102K	4- 61	AA		C	
〃	6- 14	AA		C	
〃	8- 11	AA		C	
VCKYTV1HB103K	4- 62	AB		C	
VCKYTV1HB153K	4- 63	AA		C	
VCKYTV1HB222K	4- 64	AA		C	
VCKYTV1HB332K	4- 65	AA		C	
VCKYTV1HB333K	4- 66	AA		C	
VCKYTV1HF104Z	4- 67	AA		C	
〃	6- 15	AA		C	
VCQYNA2AM103K	4- 68	AA		C	
VHD1SR159//-1	4- 69	AF		B	
VHD1SS353//-1	4- 70	AB		B	
〃	6- 16	AB		B	
VHDCP301///-1	4- 71	AL		B	
VHDRB160L-401	4- 72	AG		B	
VHDSFPB54//-1	8- 12	AC		B	
VHEMTZ5.1A/-1	4- 73	AC		B	
VHEPTZ30B++-1	4- 74	AG	N	B	
VHEPTZ5.6B/-1	4- 75	AG		B	
VHEUDZ33B//-1	4- 76	AC		B	
VHi2032ARAB1A	4- 77	AZ		B	
VHi27256RDH1A	4- 97	AW		B	
VHi28F016SU70	4- 78	BR		B	
VHi4M16SŌJ60/	4- 79	AV		B	
VHi51V8512T12	4- 80	BG		B	
VHi74AHCT245D	4- 81	AP		B	
VHi74HC138DR/	6- 17	AK		B	
VHi74LV08/DR/	4- 82	AK		B	
VHi74LV138DR/	4- 83	AP		B	
VHi74LV14ADR/	4- 84	AM		B	
VHi74LVX00/SJ	4- 85	AL		B	
VHi74LVX08/SJ	4- 86	AG		B	
VHi74LVX32/SJ	4- 87	AL		B	
VHiBA10339F-1	4- 88	AD		B	
VHiBA10393F-1	4- 89	AC		B	
VHiBR6265BF10	4- 90	AR		B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VHiH4728B02FS	6- 18	AW		B	
VHiH641510810	4- 91	BA		B	
VHiKiA7045F-1	4- 92	AL	N	B	
VHiKiA7806P-1	4- 93	AK		B	
VHiL4960V//-1	4- 94	AS		B	
VHiLT1184CS-1	8- 13	BE		B	
VHiLZ9FK13/-1	4- 95	BA		B	
VHiLZ9FT18/-1	4- 96	AZ		B	
VHiMB62H149-1	4- 98	BC		B	
VHiMC145406F1	4- 99	AL		B	
VHiMC68B54/-1	4-100	BB		B	
VHiMN89303/-1	4-101	BD		B	
VHiRH5RE33A-1	4-102	AF		B	
VHiSN74HC00DR	4-103	AG		B	
VHiSN74HC04DR	4-104	AG		B	
VHiSN74HC08DR	4-105	AL		B	
VHiSN74HC153D	6- 19	AK		B	
VHiSN74HC74D1	4-106	AG		B	
VHiSN74HCU04D	4-107	AG		B	
VHiSN74LS125R	6- 20	AL		B	
VHiSN75115NS1	4-108	AN		B	
VHiSN75189DR/	4-109	AK		B	
VHiTA79L024-1	4-110	AE	N	B	
VHiTD62308F-1	4-111	AH		B	
VHiUPD71037GB	4-112	AY		B	
VHiZ84C0006FE	4-113	AT		B	
VHiZ84C3006FE	4-114	AT		B	
VHViCPS0.5/-1	8- 14	AF		B	
VHViCPS1.0/-1	4-115	AF		B	
VRD-RB2HY394J	7- 8	AA		C	
VRD-RC2EY221J	4-116	AA		C	
VRS-RE3AAR39J	4-117	AB		C	
VRS-RE3LA151J	4-118	AC		C	
VRS-TS2AD000J	4-119	AA		C	
VRS-TS2AD101J	4-120	AA		C	
VRS-TS2AD102J	4-121	AA		C	
VRS-TS2AD103J	4-122	AA		C	
VRS-TS2AD104J	4-123	AA		C	
〃	8- 15	AA		C	
VRS-TS2AD105J	4-124	AA		C	
〃	6- 21	AA		C	
VRS-TS2AD112J	4-125	AA		C	
VRS-TS2AD122J	4-126	AA		C	
VRS-TS2AD123J	4-127	AA		C	
VRS-TS2AD143F	4-128	AB		C	
VRS-TS2AD152G	4-129	AA		C	
VRS-TS2AD153G	4-130	AA		C	
VRS-TS2AD162J	4-131	AA		C	
VRS-TS2AD222J	4-132	AA		C	
VRS-TS2AD224J	8- 16	AA		C	
VRS-TS2AD272J	4-133	AA		C	
VRS-TS2AD302J	4-134	AA		C	
VRS-TS2AD303F	4-135	AA		C	
VRS-TS2AD330J	4-136	AA		C	
VRS-TS2AD332F	8- 17	AA		C	
VRS-TS2AD392G	4-137	AA		C	
VRS-TS2AD432J	4-138	AA		C	
VRS-TS2AD470J	4-139	AA		C	
VRS-TS2AD472F	4-140	AA		C	
VRS-TS2AD472J	4-141	AA		C	
〃	6- 22	AA		C	
〃	8- 18	AA		C	
VRS-TS2AD473J	4-142	AA		C	
〃	6- 23	AA		C	
VRS-TS2AD512F	4-143	AA		C	
VRS-TS2AD513J	4-144	AA		C	
VRS-TS2AD561J	4-145	AA		C	
VRS-TS2AD562J	4-146	AA		C	
VRS-TS2AD563J	4-147	AA		C	
VRS-TS2AD622F	4-148	AA		C	
VRS-TS2AD681J	4-149	AA		C	
VRS-TS2AD751J	8- 19	AA		C	
VRS-TS2AD822G	8- 20	AA	N	C	
VRS-TS2AD912G	4-150	AA		C	
VRS-TS2HD122J	4-151	AC		C	
VRS-TS2HD130J	4-152	AD		C	
VS2SA1270-/-1	4-153	AF		B	
VS2SC4699KP-1	4-154	AC		B	
VS2SC5001R/-1	8- 21	AF		B	
VS2SJ187-//-1	4-155	AF		B	
VSDTA144EK/-1	4-156	AC		B	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VSDTC114YK/-1	4-157	AC		B	
〃	6- 24	AC		B	
VSKTA1273//-1	4-158	AF		B	
VSKTC3199//-1	4-159	AC	N	B	
VSKTD1413++-1	4-160	AN	N	B	
VVLLM320153-1	1-502	BW		E	
【X】					
XBBSD30P04000	2- 15	AA		C	
XBBSD30P06000	1- 28	AA		C	
XBBSD30P08KS0	2- 18	AA		C	
XBBSD40P12000	1- 5	AA		C	
XBPBZ40P06K00	2- 13	AA		C	
XBPSD30P06000	4-161	AA		C	
XBPSD30P06K00	2- 9	AA		C	
XEBSD30P06000	1- 44	AA		C	
〃	2- 3	AA		C	
XEBSD30P08000	1- 13	AA		C	
〃	2- 11	AA		C	
XEBSD30P10000	1- 14	AA		C	
〃	2- 36	AA		C	
XEBSF30P08000	1- 35	AA		C	
XEPSD30P10000	2- 50	AA		C	
XHBSD30P04000	1- 38	AA		C	
〃	2- 2	AA		C	
XJPSD30P05000	1- 51	AA		C	
XJSSD26P08000	1- 33	AA		C	
XJSSD30P08000	2- 62	AA		C	
XJSSF30P12000	2- 28	AB		C	
XUPSD40P12000	2- 34	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	

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